2026 IEEE 18th International Conference on Solid-State and Integrated Circuit Technology

October 27 - 30, 2026 Hangzhou, China

CONFERENCE PROGRAM



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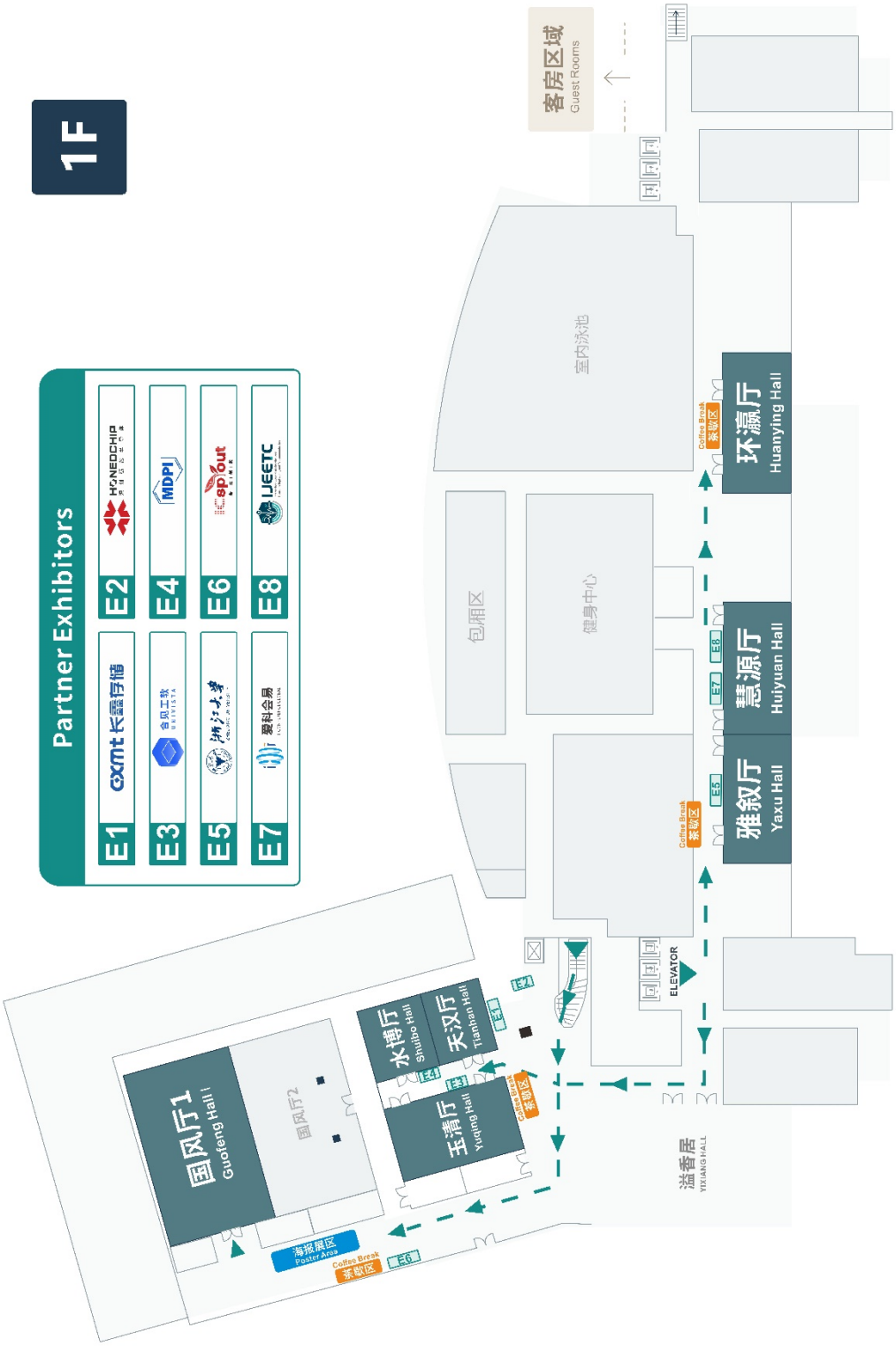
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Conference Venue

Hangzhou Blossom Water Museum Hotel (杭州宝盛水博园大酒店)

Address: No.118 Shuibo Road, Xiaoshan District, Hangzhou, China

地址：杭州市萧山区宁围街道水博大道 118 号




2F
Partner Exhibitors
E1
E2
E3
E4
E5
E6
E7
E8
海纳
Haina
客房区域
Guest Rooms
主题背景板
Conference Backdrop
签到处
Registration
酒店入口
HOTEL ENTRANCE
Front Desk
Elevator
玉玲珑
古越厅
清莲厅
Qinglian Hall
宝盛厅
Blossom Hall
Coffee Break
茶歇区

Conference Guideline

About Presentation

- Presentation Duration: The duration for a **plenary speech** is 40 minutes, a **keynote presentation** is 30 minutes, an **invited presentation** is 20 minutes, and **an oral presentation** is 15 minutes. Please target your lecture for a duration of about 3 minutes for questions from the audience.
- Your punctual arrival and active involvement in each session will be highly appreciated.
- Get your presentation PPT or PDF files prepared and backed up.
- Laptops(except competition session), projector & screen, laser sticks will be provided by the conference organizer.

Poster Presentation

It's expected that at least one author stands by the poster for (most of the time of) the duration of the poster session. Thumb pins, adhesive tapes, and scissors will be provided at the poster area. The poster should be taken off by 21: 30 by the author if he or she would like to keep it. After that time, it will be removed and be regarded as being discarded by the authors.

Security

Please ensure that you take your belongings with you at all times when leaving a room. Do not leave bags or laptops unattended.

Name Badge

For security purposes, delegates, speakers, exhibitors and staff are required to wear their name badge to all sessions and social functions. Entrance into sessions is restricted to registered delegates only. If you misplace your name badge, please replace at the registration counter.

Catering

Haina：海纳自助餐厅（2F）

Conference Rooms

1F

Yaxu Hall：雅叙厅

Huiyuan Hall：慧源厅

Huanying Hall：环瀛厅

Yuqing Hall：玉清厅

Shuibo Hall：水博厅

Tianhan Hall：天汉厅

Guofeng Hall I：国风厅 1

2F

Blossom Hall：宝盛厅

Qinglian Hall：清莲厅

Conference Registration

Venue

Lobby of Hangzhou Blossom Water Museum Hotel

Time

Oct. 27: 10:00-19:00　Oct. 28: 08:00-18:00

Oct. 29: 08:00-18:00　Oct. 30: 08:00-17:00

Conference Photos

Conference Program

Agenda Overview

October 27, 2026

Time	Activities	Venue
14:00-17:00	**Tutorial 01:** AI-Driven Modular Designs and Optimizations for RFICs	Huiyuan Hall
	Tutorial 02: Smart Sensing SoCs Based on Heterogeneous CMOS-MEMS Integration and Sensor-AI Co-Designed Architectures	Yaxu Hall
14:00-15:30	**Tutorial 04:** Artificial Intelligence for 6G: Implementations, Algorithms, and Optimizations	Yuqing Hall
16:00-17:30	**Tutorial 03:** Breaking the AI-Computing Driven Interconnect Bottleneck	
14:00-17:00	**Tutorial 05:** Advanced Memory Systems: Reliable Storage and Efficient Computing	Huanying Hall
14:00-15:30	**Analog Competition Topic:** AI Agent-Based Automatic Optimization Design of FVF LDO	Shuibo Hall
15:30-17:00	**Digital Competition Topic:** AI Agent-Based NPU Design and Verification	
18:00-20:30 / Welcome Reception @Haina		

October 28, 2026

Time	Activities	Venue
09:00-09:30	**Opening Ceremony**	Blossom Hall
	Host: **Yuehang Xu,** *University of Electronic Science and Technology of China, China*	
	Plenary Speech	Blossom Hall
	Host: **Cor Claeys,** *KU Leuven, Belgium*	
09:30-10:10	Plenary Speaker: **Paul Penzes,** *Qualcomm Technologies, USA* **Speech Title:** Engineering the Future: How AI Is Transforming Hardware Design	
10:10-10:30 / Coffee Break		
10:30-11:10	Plenary Speaker: **Mohamad Sawan,** *IEEE Life Fellow, Westlake University, China* **Speech Title:** Systems-on-Chips BCI-based Neuromodulation to Learn, Treat and Predict Brain Diseases	
	Plenary Speeches	Blossom Hall
	Host: **Cheng Zhuo,** *Zhejiang University, China*	
11:10-11:50	Plenary Speaker: **Zhongfeng Wang,** *IEEE, AAIS Fellow, Sun Yat-sen University, China* **Speech Title:** Computation-Aware Optimization and Multi-Concurrency Architecture Design for Lattice-Based Post-Quantum Cryptography Hardware	

11:50-12:30	Plenary Speaker: **Wai Tung Ng,** *University of Toronto, Canada* **Speech Title:** Powering AI Data Centers-Opportunities for Advanced Packaging, Power Semiconductors and ICs	
12:30-13:30 / Lunch @Haina		
13:30-15:30	**Special Session 1:** Ferroelectric Materials and Devices-I	Guofeng Hall I
	Special Session 2: Oxide Semiconductor Devices-I	Qinglian Hall
	Technical Session 01: General Analog-I	Huanying Hall
	Technical Session 02: Power Devices & Power IC-I	Yuqing Hall
	Technical Session 03: RF & Wireless-I	Huiyuan Hall
	Technical Session 04: Semiconductor Process Technologies-I	Yaxu Hall
	Technical Session 05: Wireline	Shuibo Hall
	Technical Session 06: Digital Circuits-I	Tianhan Hall
15:30-16:00 / Coffee Break		
15:30-16:00	**Poster Session 01**	Foyer (1F)
15:45-18:15	**Outstanding Young Scholar Award Session**	Guofeng Hall I
16:00-18:00	**Technical Session 07:** Device Reliability & Security-I	Qinglian Hall
	Technical Session 08: Design Methodology & EDA-I	Huanying Hall
	Technical Session 09: Power Devices & Power IC-II	Yuqing Hall
	Technical Session 10: Digital Architectures & Systems-I	Huiyuan Hall
	Technical Session 11: CMOS Logic Devices & Sensors-I	Yaxu Hall
	Technical Session 12: Optoelectronics and Silicon Photonics Integration-I	Shuibo Hall
	Technical Session 13: Packaging Technologies	Tianhan Hall
18:30-20:30 / Banquet @Blossom Hall		

October 29, 2026

Time	Activities	Venue
	Plenary & Keynote Speeches	Blossom Hall
	Host: **Amara Amara,** *International Innovation Institute, Beihang University, Hangzhou Campus, China*	
09:00-09:40	Plenary Speaker: **Hanming Wu,** *Academician of the Chinese Academy of Engineering, Zhejiang University, China* **Speech Title:** AI-IC Mutual Empowerment in the Information Era: Recent Progress from Zhejiang University's Public Pilot Platform	
09:40-10:20	Plenary Speaker: **Jianjun Luo,** *Hangzhou Dianzi University, China* **Speech Title:** Non-Volatile Memory Technology & Application Trends in Industry	
10:20-10:50 / Coffee Break		
10:50-11:30	Plenary Speaker: **Zewen Liu,** *Tsinghua University, China* **Speech Title:** GaN-MEMS Sensor and Its Application	
11:30-12:00	Keynote Speaker: **Mingyuan Liu,** *CXMT Corporation, China* **Speech Title:** Technology Breakthrough in DRAM Evolution with Innovative Solutions	
12:00-13:30 / Lunch @Haina		
13:30-15:30	**Special Session 1:** Ferroelectric Materials and Devices-II	Guofeng Hall I
	Special Session 2: Oxide Semiconductor Devices-II	Qinglian Hall
	Technical Session 14: General Analog-II	Huanying Hall
	Technical Session 15: Power Devices & Power IC-III	Yuqing Hall
	Technical Session 16: CMOS Logic Devices & Sensors-II	Huiyuan Hall
	Technical Session 17: Device Reliability & Security-II	Yaxu Hall
	Technical Session 18: RF & Wireless-II	Shuibo Hall
	Technical Session 19: Digital Architectures & Systems-II	Tianhan Hall
15:30-16:00 / Coffee Break		
15:30-16:00	**Poster Session 02**	Foyer (1F)
16:00-18:00	**Special Session 1:** Ferroelectric Materials and Devices-III	Guofeng Hall I
	Technical Session 20: Optoelectronics and Silicon Photonics Integration-II	Qinglian Hall
	Technical Session 21: Design Methodology & EDA-II	Huanying Hall
	Technical Session 22: Power Devices & Power IC-IV	Yuqing Hall
	Technical Session 23: CMOS Logic Devices & Sensors-III	Huiyuan Hall
	Technical Session 24: Device Reliability & Security-III	Yaxu Hall
	Technical Session 25: Semiconductor Process Technologies-II	Shuibo Hall
	Technical Session 26: Digital Circuits-II	Tianhan Hall
18:00-20:00 / Dinner @Haina		

October 30, 2026

Time	Activities	Venue
09:00-10:15	**Special Session 1:** Ferroelectric Materials and Devices-IV	Guofeng Hall I
	Special Session 3: Advanced Memory and Computing-In-Memory Circuit Design	Shuibo Hall
	Technical Session 27: General Analog-III	Qinglian Hall
	Technical Session 28: CMOS Logic Devices & Sensors-IV	Huanying Hall
	Technical Session 29: Power Devices & Power IC-V	Yuqing Hall
	Technical Session 30: Design Methodology & EDA-III	Huiyuan Hall
	Technical Session 31: Device Reliability & Security-IV	Yaxu Hall
	Technical Session 32: Digital Architectures & Systems-III	Tianhan Hall
10:15-10:45 / Coffee Break		
10:15-10:45	**Poster Session 03**	Foyer (1F)
10:45-12:00	**Special Session 1:** Ferroelectric Materials and Devices-V	Guofeng Hall I
	Technical Session 33: General Analog-IV	Qinglian Hall
	Technical Session 34: CMOS Logic Devices & Sensors-V	Huanying Hall
	Technical Session 35: Power Devices & Power IC-VI	Yuqing Hall
	Technical Session 36: Design Methodology & EDA-IV	Huiyuan Hall
	Technical Session 37: Device Reliability & Security-V	Yaxu Hall
	Technical Session 38: Power Devices & Power IC-VII	Shuibo Hall
	Technical Session 39: RF & Wireless-III	Tianhan Hall
12:00-13:30 / Lunch @Haina		
13:30-15:30	**Special Session 1:** Ferroelectric Materials and Devices-VI	Guofeng Hall I
	Technical Session 40: General Analog-V	Qinglian Hall
	Technical Session 41: CMOS Logic Devices & Sensors-VI	Huanying Hall
	Technical Session 42: Power Devices & Power IC-VIII	Yuqing Hall
	Technical Session 43: Design Methodology & EDA-V	Huiyuan Hall
	Technical Session 44: Device Reliability & Security-VI	Yaxu Hall
	Technical Session 45: Power Devices & Power IC-IX	Shuibo Hall
	Technical Session 46: RF & Wireless-IV	Tianhan Hall
15:30-16:00 / Coffee Break		
15:30-16:00	**Poster Session 04**	Foyer (1F)
16:00-18:00	**Technical Session 47:** Power Devices & Power IC-X	Guofeng Hall I
	Technical Session 48: General Analog-VI	Qinglian Hall
	Technical Session 49: CMOS Logic Devices & Sensors-VII	Huanying Hall
	Technical Session 50: Power Devices & Power IC-XI	Yuqing Hall
	Technical Session 51: RF & Wireless-V	Huiyuan Hall

16:00-18:00	**Technical Session 52:** Device Reliability & Security-VII	Yaxu Hall
	Technical Session 53: Semiconductor Process Technologies-III	Shuibo Hall
	Technical Session 54: Digital Architectures & Systems-IV	Tianhan Hall
18:00-19:30 / Dinner @Haina		

Plenary Speakers

Time	09:30-10:10, October 28, 2026
Venue	Blossom Hall



Paul Penzes

Qualcomm Technologies, USA

Bio.: Paul Penzes is Vice President of Engineering at Qualcomm Technologies, where he leads global teams across design technology, foundation IP, and computer-aided design. With more than 20 years of experience spanning the full ASIC and SoC engineering lifecycle, Paul has helped deliver advanced technology and methodology solutions into high-volume products on demanding schedules. Throughout his career, Paul has focused on improving engineering productivity and design quality through innovation in methodology, infrastructure, and optimization. His areas of expertise include power, performance, and area optimization; design and CAD methodology; strategic technology planning; and execution across complex, multi-business-unit engineering programs. Before joining Qualcomm, Paul held technical leadership roles at Broadcom, where he served as Associate Technical Director and Distinguished Engineer in the Office of the CTO, and at Myricom as a Senior VLSI Engineer. Paul earned his PhD in Computer Science from Caltech, where his thesis, Energy-Delay Complexity of CMOS Circuits, explored the theoretical foundations of energy and performance tradeoffs in CMOS circuit design. He also holds a master's degree in Computer Science and a bachelor's degree in Engineering and Applied Sciences from Caltech.

Engineering the Future: How AI Is Transforming Hardware Design

Abstract: Artificial Intelligence is reshaping the way complex hardware systems are conceived, designed, verified, and optimized. As semiconductor technologies continue to advance and design complexity grows exponentially, traditional engineering approaches are increasingly complemented by AI-driven techniques that accelerate innovation and improve productivity. From functional verification and uncovering hard-to-find defects to enabling rapid design space exploration, optimization, and predictive insights, AI is helping engineering teams solve increasingly complex problems faster and more effectively than ever before. This presentation explores the rapidly evolving role of AI across the hardware development lifecycle, highlighting real-world applications, emerging methodologies, and measurable business impact. Attendees will learn how machine learning, generative AI, and data-driven automation are reducing design turnaround times, improving quality of results, and augmenting engineering decision-making. The session will also discuss organizational considerations, including token usage, workflow integration, and the evolving role of engineers in an AI-enabled design environment.

Plenary Speakers

Time	10:30-11:10, October 28, 2026
Venue	Blossom Hall



Mohamad Sawan

IEEE Life Fellow
Westlake University, China

Bio.: Mohamad Sawan (Life Fellow, IEEE) received the Ph.D. degree from the University of Sherbrooke, Canada. He is currently a Chair Professor with Westlake University, Hangzhou, China, and an Emeritus Professor with Polytechnique Montreal, Canada. He is the Founder and the Director of the Centre of Excellence in Biomedical Research of Advanced Integrated-on-chips Neurotechnologies (CenBRAIN Neurotech), Westlake University, and the Polystim Neurotech Laboratory, Polytechnique Montreal. He has published over 1000 peer-reviewed papers, five books, 15 book chapters, and 15 awarded and 25 pending patents. He is a fellow of Canadian Academy of Engineering and the Engineering Institutes of Canada and an Officer of the National Order of Quebec. He received several awards, including the Queen Elizabeth II Golden Jubilee Medal, the Shanghai International Collaboration Award, the Zhejiang Westlake Friendship Award, the Qianjiang Friendship Ambassador Award, and the Medal of Merit from the President of Lebanon. He is the Founder of the Polystim Neurotech Laboratory and the Co-Founder of International IEEE-NEWCAS and International IEEE-BioCAS Conference. He was the General Chair of 2016 IEEE International Symposium on Circuits and Systems, and 2020 IEEE International Medicine, Biology, and Engineering Conference (EMBC). He was the Canada Research Chair in Smart Medical Devices (2001-2015), and led the Microsystems Strategic Alliance of Quebec, Canada (1999-2018). He was a VP of Publications of IEEE Circuits and Systems Society, from 2019 to 2022. He is a Co-Founder and an Associate Editor of IEEE Transactions on Biomedical Circuits and Systems. He was the Editor-in-Chief of IEEE Transactions on Biomedical Circuits and Systems, from 2016 to 2019.

Systems-on-Chips BCI-based Neuromodulation to Learn, Treat and Predict Brain Diseases

Abstract: Systems-on-Chips brain-computer Interfaces for efficient neuromodulation are promising approaches to make a difference on sensing, treatment and prediction of complex Neurodegenerative diseases. Neuroelectronic' approaches are facilitating the emergence of these closed-loop neuromodulation, which requires fast and very low-power miniaturized systems when are intended to reside within the skull. Implemented to continuously operate without stop, these devices contain large channel counts to record neural activities and to microstimulate tissues to re-activate functions or to stop non desired events such as seizures. We cover in this talk multimodal interfaces and implantable platforms grouping various biosensing techniques and other massively parallel neurorecording channels, as well as corresponding neuromorphic processing engines. We deal with multidimensional design challenges such as miniaturisation, reliability, safety, self-powered operation, and harvesting power and high-data rate wireless communication. Case studies will include Epilepsy, Addictions, Vision, and Language decoding.

Plenary Speakers

Time	11:10-11:50, October 28, 2026
Venue	Blossom Hall



Zhongfeng Wang

IEEE, AAIS Fellow
Sun Yat-sen University, China

Bio.: Dr. Zhongfeng Wang (Fellow, IEEE and AAIS) received the B.S. and M.S. degrees from Tsinghua University, Beijing, China, and the Ph.D. degree from the University of Minnesota, Minneapolis, USA, in 2000. He previously worked for National Semiconductor Corporation, Oregon State University, and Broadcom Corporation, where he served as Senior Principal Scientist and Technical Director, successively. In 2016, he joined Nanjing University, China, as Distinguished Professor and Deputy Dean of the School of Microelectronics. In 2023, he joined Sun Yat-sen University, China, where he currently serves as Dean of the School of Integrated Circuits. He is also a National Distinguished Expert and Editor-in-Chief of the Journal of the International Academy of Artificial Intelligence Sciences (JAAIS). Dr. Wang has deeply participated in more than 10 commercial chip designs with a cumulative revenue of over $1B. He has published over 500 technical papers and holds more than 100 U.S. and China granted patents. He has received nine best paper awards from major IEEE conferences and transactions in the related fields of Integrated Circuits, including the IEEE Circuits and Systems Society (CASS) VLSI Transactions Best Paper Award in both 2007 and 2025. Moreover, he has made significant contributions on many industrial standards. So far, his technical proposals have been adopted by more than 20 international networking standards. His current research interests include high-speed communications, artificial intelligence, and low-power VLSI design.

Computation-Aware Optimization and Multi-Concurrency Architecture Design for Lattice-Based Post-Quantum Cryptography Hardware

Abstract: Quantum computing drives a paradigm shift in public-key cryptography. NIST's 2024 ML-KEM and ML-DSA standards mark a transition in lattice-based PQC from algorithmic design to large-scale deployment across communication, cloud, and embedded systems-a shift that hinges on hardware acceleration. General-purpose optimizations fail to exploit the underlying computation structure, causing circuit redundancy, resource imbalance, and wasted concurrency. This talk introduces two complementary approaches: (1) computation-aware optimizations, exploiting algebraic properties, statistical traits, self-similarity, and physical constraints, yielding a fine-grained decomposed modular multiplier, an addition-only NTT, reconfigurable datapaths built on normalized computational forms, and near-memory redundant arithmetic; (2) architecture-aware parallel computing, utilizing algorithmic retiming, algorithm-level look-ahead, and multi-issue scheduling to boost concurrency and compute density across pure-hardware, HW/SW co-design, and compute-in-memory architectures. These schemes should offer a good reference for hardware design in lattice-based cryptography and broader lattice-structured computation.

Plenary Speakers

Time	11:50-12:30, October 28, 2026
Venue	Blossom Hall



Wai Tung Ng

University of Toronto, Canada

Bio.: Wai Tung Ng received his B.A.Sc., M.A.Sc., and Ph.D. degrees in Electrical Engineering from the University of Toronto, in 1983, 1985 and 1990, respectively. Prof. Ng is with the Edward S. Rogers Sr. Dept. of Electrical and Computer Engineering, University of Toronto. He is also the director of the Toronto Nanofabrication Center (TNFC). Prof. Ng is an active researcher in the areas of power semiconductor devices and smart power integrated circuits. Currently, Prof. Ng's group is actively promoting the co-design of smart gate driver ICs and advanced packaging techniques for the implementation of liquid-cooled intelligent power modules (IPMs).

Powering AI Data Centers-Opportunities for Advanced Packaging, Power Semiconductors and ICs

Abstract: The rapid expansion of AI and high-performance computing is driving a fundamental transformation of data center power delivery from the grid down to sub 1 V chip-level loads. This not only imposes unprecedented requirements on power semiconductor devices and packaging technologies but also offers great opportunities. This talk presents an end-to-end view of the evolving power delivery network, spanning medium-voltage grid interfaces, solid-state transformers, 800-1500 VDC microgrids, energy storage systems, intermediate bus architectures, and final point-of-load conversion. Wide-bandgap devices, particularly SiC and GaN, are enabling higher efficiency, switching speed, and power density across these stages; however, their full potential is realized only through advanced gate driving and packaging innovations that minimize parasitics, enhance thermal management, and support high voltage and high frequency operation. Key trends include low-inductance module design, embedded and co-packaged power stages, integrated magnetics, and direct liquid cooling, as well as the transition toward vertical power delivery and heterogeneous integration at the chip level. Ultimately, the co-optimization of devices, packaging, and system architectures is essential to meet the efficiency, scalability, and reliability demands of next-generation data centers.

Plenary Speakers

Time	09:00-09:40, October 29, 2026
Venue	Blossom Hall



Hanming Wu

Academician of the Chinese Academy of Engineering
Zhejiang University, China

Bio.: Hanming Wu, Professor/Academician of the Chinese Academy of Engineering, expert in IC process for manufacturing. He got his PhD degree from Chinese Academy of Sciences in 1987. Following his doctoral studies, he joined in postdoctoral research at the UT Austin and the UC Berkeley, USA. After that, he worked as a senior process development engineer at Novellus and Intel in California. Since 2001, he joined SMIC and led the development of China's VLSI process technology from 0.13um to 14nm. Throughout his career, he has dedicated himself to advance the IC fabrication technology of China. As the principal investigator, he has won three times of 2nd prizes for National Scientific and Technological Progress. In 2014, he was honored with the title of "Top Ten Outstanding National Science and Technology Workers". He has published 116 papers and holds 67 licensed invention patents. In 2019, he was elected as an academician of the Chinese Academy of Engineering and currently serves as the Dean of the College of Integrated Circuits at Zhejiang University. After setting up an IDM-like 55nm CMOS public platform in the university, his current research interests include virtual and intelligent IC manufacturing, DTCO, and emerging technology transformation based on the platform.

AI-IC Mutual Empowerment in the Information Era: Recent Progress from Zhejiang University's Public Pilot Platform

Abstract: Artificial intelligence (AI) is reshaping integrated circuit (IC) manufacturing and design by enabling more efficient, accurate, and autonomous technology development. At the same time, the rapid growth of AI is creating strong demands for new semiconductor solutions, including high-performance computing, energy-efficient devices, emerging memories, and specialized hardware accelerators. This talk presents recent progress from Zhejiang University's 12-inch CMOS public pilot line platform, which provides a closed-loop environment connecting virtual manufacturing, AI-enhanced EDA, IC design, fabrication, and hardware development for AI applications.

Based on unified manufacturing datasets and a dedicated data infrastructure, the platform supports virtual fabrication, intelligent process optimization, and large-model-based design-technology co-optimization. Several AI-driven applications have been developed, including Domain-Specific Large Language Model, Virtual Fab, etc. On the hardware side, recent advances such as CMOS-synapse-based fully analog neural-network chips, low-temperature CMOS technologies for energy-efficient AI accelerators, and application-specific AI power-delivery solutions for chiplet systems further demonstrate the expanding synergy between IC and AI. These efforts highlight the critical role of public pilot platforms in accelerating AI – IC mutual empowerment and semiconductor innovation.

Plenary Speakers

Time	09:40-10:20, October 29, 2026
Venue	Blossom Hall



Jianjun Luo

Hangzhou Dianzi University, China

Bio.: Jianjun (Jerome) Luo, the Dean of Microelectronic Research Institute in Hangzhou Dianzi University, also the founder and CTO of Sage Microelectronics. He earned a PhD in semiconductor technology from Zhejiang University in China, a Master's in Microelectronics from the Hangzhou Dianzi University, and a Bachelor's in Electronics Engineering from Shanghai Jiao Tong University. He accumulated his experience in communication and storage IC design for more than 30 years. He won the second prize of National Scientific and Technological Progress Award, and Ho Leung Ho Lee Foundation's Scientific and Technological Award.

Non-Volatile Memory Technology & Application Trends in Industry

Abstract: Flash memory is the most popular Non-Volatile memory in data storage industry. It is facing challenge of reliability and endurance when going to the next generation with the most advanced semiconductor process. Flash memory controller should take actions to clean the issues for the next generation Solid-State Drive with Flash Memory. At the same time, new memory devices, such as RRAM, MRAM and FeRAM, are exploring their niche market. However, these new memory technologies have to make trade-off to satisfy the unique applications. This plenary speech is going to allocate these memory devices in dedicated applications according to their advantages and disadvantages.

Plenary Speakers

Time	10:50-11:30, October 29, 2026
Venue	Blossom Hall



Zewen Liu

Tsinghua University, China

Bio.: Prof. Dr. Zewen LIU, he graduated from Physics department of University of Science and Technology of China and obtained a doctoral degree from Paris XI University (Now Université Paris-Saclay) in France. He worked on microelectronics process and devices in the Institute of Microelectronics (now the School of Integrated Circuits) at Tsinghua University since 1997. He has been engaged in integrated circuit technology, nanofabrication technology, MEMS and sensor research and make important contribution to photolithography technology, RF MEMS devices, silicon-based solid-state nanopores, and gallium nitride MEMS sensors and won the Best Paper Award of the China Electronics Society, the International IEEE Best Paper Nomination Award, as well as titles such as Suzhou Leading Talent, Tsinghua Excellent Teacher, and Excellent Doctoral Supervisor. He has published over 200 academic papers, applied for and obtained nearly 100 patent authorizations, translated two academic books, and contributed important chapters in two English works. He has visited European universities multiple times for academic exchanges and lectures, and has served as the executive chairman of the China Netherlands Semiconductor High level Talent Forum Summer School for several consecutive years.

GaN-MEMS Sensor and Its Application

Abstract: The MEMS sensor based on 2DEG (Two-Dimensional Electron Gas) formed within wide bandgap semiconductor GaN/AlGaN heterojunction and its applications will be presented in this talk. After the introduction and a brief explanation of the principle of GaN/AlGaN 2DEG as sensing structure, a researches and fabrications of novel Gallium Nitride sensor devices is reviewed, which includes ultraviolet sensors, Hall sensors, gas sensors, biosensors and other sensors. At the end we will discuss the future intelligent sensors and the application of artificial intelligence in sensor systems.

Keynote Speakers

Time	11:30-12:00, October 29, 2026
Venue	Blossom Hall



Mingyuan Liu

CXMT Corporation, China

Bio.: Dr. Mingyuan Liu, PhD in Materials Science from Shanghai Jiao Tong University in 2004. With 22 years of experience in the research and development of integrated process technology, he mainly focuses on technology development on advanced Logic, DRAM and NAND. Having worked in memory technology research and development for many years, he is currently the vice president of CXMT Corporation, the head of Technology Center of Excellence. Additionally, he serves as the Executive Director of the Chinese Institute of Electronics (CIE) and a Standing Member of Academic Committee in the National Center of Technology Innovation for EDA. He has published nearly 20 technical papers and holds over 45 patents in both China and the United States.

Technology Breakthrough in DRAM Evolution with Innovative Solutions

Abstract: The rapid development of AI technology has catalyzed immense demand in the memory market. DRAM serves as the optimal solution to meet the memory requirements, ensuring high-speed and high-bandwidth data interaction between the CPU/GPU and external systems.

This report will present a comparative analysis between DRAM and logic process technologies, highlighting the technical challenges inherent in DRAM fabrication. Furthermore, utilizing the CXMT's 5th generation process platform as a case study, it provides an in-depth analysis of the manufacturing complexities and innovative solutions associated with DRAM. Finally, a comprehensive overview of the CXMT latest products will be presented.

Track 1: Digital Architectures & Systems



Fakhrul Zaman Rokhani
Universiti Putra Malaysia,
Malaysia

Track 2: Digital Circuits



Philippe Royannez
MaxLinear, Inc.,
United States

Track 3: Design Methodology & EDA



Xiaohang Wang
Zhejiang University, China

Track 4: RF & Wireless



Zhe Liu
Tianjin University, China



Chun Wang
Zhejiang University, China

Track 7: CMOS Logic Devices & Sensors



Hailin Peng
Peking University, China



Linxi Dong
Hangzhou Dianzi University, China

Track 9: Device Reliability & Security



Yuhao Zhang
The University of Hong Kong, China

Special Session 1: Ferroelectric Materials and Devices



Qianqian Huang
Peking University, China



Xiaolei Wang
Institute of Microelectronics, CAS, China



Hangbing Lv
Xiamen University, China

Special Session 2: Oxide Semiconductor Devices



Guilei Wang
Beijing Superstring Academy of Memory Technology, China



Chuan Liu
Sun Yat-Sen University, China

Invited Speakers

Track 1: Digital Architectures & Systems



Letian Huang
UESTC Yangtze Delta Region Institute, China

Track 4: RF & Wireless



Geliang Yang
Guangdong University of Technology, China



Kai Li
Tianjin University, China



Liang Gao
Southeast University, China



Bingzheng Yang
Shenzhen University, China



Francois Rivet
University of Bordeaux, France

Track 5: Wireline



Zhao Zhang
Institute of Semiconductors, CAS, China

Track 6: General Analog



Zhuojun Chen
Hunan University, China



Run Min
Huazhong University of Science and Technology, China



Jian Zhao
Shanghai Jiao Tong University, China



Zhong Tang
Hangzhou Institute of Technology, Xidian University, China

Track 7: CMOS Logic Devices & Sensors



Hua Fan
University of Electronic Science and Technology of China, China



Han Li
Southeast University, China



Jiezhi Chen
Shandong University, China



Junwei Luo
Institute of Semiconductors, CAS, China



Ran Cheng
Zhejiang University, China



Jun Luo
Institute of Microelectronics, CAS, China



Liang Ran
Pixelcore, China



SangHoon Shin
Hanyang University, South Korea

Track 8: Power Devices & Power IC



Yawei Chen
China Resources Microelectronics Ltd., China



Jie Wei
University of Electronic Science and Technology of China, China



Wen Yang
South China University of Technology, China



Guoliang Yao
Hangzhou Silan Microelectronics Co., Ltd., China



Yang Liu
Xidian University, China



Kemeng Yang
Nanjing University of Posts and Telecommunications, China



Huaxing Jiang
South China University of Technology, China



Wei Huang
Jiangnan University, China



Qimeng Jiang
Southwest Jiaotong University, China



Xin Zhou
University of Electronic Science and Technology of China, China



Denggui Wang
Nanjing Electronic Devices Institute, China



Hao Yuan
Xidian University, China



Zhong Chen
The Hong Kong Polytechnic University, China

Track 9: Device Reliability & Security



Xuanze Zhou
University of Science and Technology of China, China



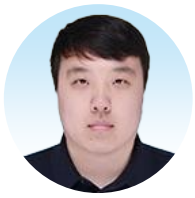
Hong Yang
Institute of Microelectronics, CAS, China



Yixu Yao
Institute of Microelectronics, CAS, China



Xiaolei Wang
Institute of Microelectronics, CAS, China



Han Yang
Peking University, China



Takuya Maeda
The University of Tokyo, Japan



Weijia Zhang
The Hong Kong University of Science and Technology, China



Chao Liu
Shandong University, China



Bin Hou
Xidian University, China

Track 10: Semiconductor Process Technologies



Niko Münzenrieder
Free University of Bozen-Bolzano, Italy

Track 11: Optoelectronics and Silicon Photonics Integration



Peng Xiao
Jiangnan University, China



Yuanfang Yu
Jiangnan University, China



Zhengjin Weng
Jiangnan University, China



Junying Li
University of Chinese Academy of Sciences, China



Tong Lin
Southeast University, China



Junyong Wang
Suzhou Institute of Nano-Tech and Nano-Bionics, CAS, China



Xuefei Li
Huazhong University of Science and Technology, China

Track 12: Packaging Technologies



Hong Xie
HuaMao Technology, China



Tian Feng
National Silicon Industry Group, China



Junjie Wang
Changjing Technology, China

Special Session 1: Ferroelectric Materials and Devices



Jiangbin Wu
Institute of Semiconductors, CAS, China



Lang Zeng
Beihang University, China



Xubing Lu
South China Normal University, China



Houfang Liu
Tsinghua University, China



Yan Cheng
East China Normal University, China



Jin Luo
Beihang University, China



Bing Chen
Xidian University, China



Xiuyan Li
Shanghai Jiao Tong University, China



Yue-Yang Liu
Institute of Semiconductors, CAS, China



Fei Mo
Beijing Institute of Technology, China



Sungjun Kim
Dongguk University, South Korea



Xiwen Liu
The Hong Kong University of Science and Technology (Guangzhou), China



Yu Zhou
Central South University, China



Jixuan Wu
Shandong University, China



Kanhao Xue
Huazhong University of Science and Technology, China



Lin Chen
Fudan University, China



Ran Cheng
Zhejiang University, China



Xunzhao Yin
Zhejiang University, China



Zhiyuan Fu
Southeast University, China



Haiwen Xu
Xidian University, China

Special Session 2: Oxide Semiconductor Devices



Yuanyuan Shi
University of Science and Technology of China, China



Chang Niu
National University of Singapore, Singapore



Ao Liu
University of Electronic Science and Technology of China, China



Yuye Kang
Huazhong University of Science and Technology, China



Fei Mo
Beijing Institute of Technology, China



Wangran Wu
Southeast University, China



Guanhua Yang
Institute of Microelectronics, CAS, China

Tutorial

Tutorial 01: AI-Driven Modular Designs and Optimizations for RFICs

14:00-17:00, October 27, 2026 @Huiyuan Hall

Tutorial Abstract

To address the critical challenges of poor design reusability and prolonged design cycle in radio frequency integrated circuit (RFIC) designs, a modular design and optimization framework is herein proposed with inspiration from the digital design methodology. For a given fabrication process node, standardized RF library cells are first constructed by virtue of an artificial intelligence (AI)-based modeling technique. Then, the set of library cells can be reused across multiple RF designs on the same process node. The AI-based library cells are trained on accurate full-wave electromagnetic (EM) data across a broad sweep of design parameters, thereby leading to parametric RF models that are virtually as accurate as the full-wave EM data. The standardized RF library cells are reusable building blocks for the construction of RF circuits, while parametric RF models provide fast and accurate performance predictions, enabling efficient design-space exploration and optimization. The parametric RF models can deliver accurate EM data within seconds, eliminating the need for time-consuming full-wave simulations at each iteration of the design optimization. This revolutionary approach to RFIC designs boosts the design efficiency by hundreds to thousands of times. As case studies, this proposed method is applied to design integrated passive device (IPD) chips. It shows that this approach can significantly improve the design efficiency and shorten the design cycle.

Tutorial Speaker(s)



Gaofeng Wang
Hangzhou Dianzi University, China

Talk Title: EMOptimizer®: An AI-Driven Modular Design and Optimization Framework for RFICs

Bio.: Gaofeng Wang received the Ph.D. degree in electrical engineering from the University of Wisconsin, Milwaukee, in 1993 and the Ph.D. degree in scientific computing from Stanford University, Stanford, California, in 2001. From 1993 to 1996, he was a Scientist at Tanner Research Inc., Pasadena, CA. From 1996 to 2001, he was a Principal Research and Development Engineer at Synopsys Inc., Mountain View, CA. In the summer of 1999, he served as a Consultant at Bell Laboratories, Murray Hill, NJ. From 2001 to 2003, he was Chief Technology Officer at Intpax, Inc., San Jose, CA. From 2004 to 2010, he was Chief Technology Officer at Siargo Inc., Santa Clara, CA. From 2010 to 2013, he was Chief Scientist at Lorentz Solution, Inc., Santa Clara, CA. From 2004 to 2013, he was also the Founding Dean and an Adjunct Professor at the Institute of Microelectronics & Information Technology, Wuhan University, Hubei, China. Since 2013, he has been a Distinguished Professor at the School of Electronics and Information, Hangzhou Dianzi University, Zhejiang, China. He has authored or co-authored 3 books and over 700 technical papers, including over 480 articles in peer-reviewed journals (such as Nature Photonics, Advanced Science, Biosensors and Bioelectronics, and IEEE Transactions), and is the holder of over 250 patents. He has been listed among the world's top 2% scientists by Stanford University since 2019. His research and development interests include integrated circuits, electromagnetics, MEMS, sensors, and nano devices. He is a Fellow of the Institution of Engineering and Technology (IET).



Yazi Cao
Hangzhou Dianzi University, China

Talk Title: AI-Driven Modular Designs and Optimizations of Integrated Passive Devices by EMOptimizer®

Bio.: Yazi Cao received the Ph.D. degree in electrical engineering from Wuhan University in 2008. He is a Distinguished Associate Professor at Hangzhou Dianzi University and an Adjunct Professor at Carleton University in Canada. He previously served for over 10 years as an Engineering R&D Design Director at a renowned overseas communications company. He is an IEEE Senior Member and a recipient of the Hangzhou Global 521 Talent Program. He has published >50 SCI-indexed papers, accumulating over 700 SCI citations and an H-index above 20, holds more than 30 authorized invention patents, and has also published a monograph titled RF Integrated Passive Device Design. He received the Hubei Province Outstanding Doctoral Dissertation Award in 2010, was a core member of the Zhejiang Province Leading Entrepreneurial and Innovation Team Award in 2019. His main research interests include RF passive integrated chip design, antenna and filter design, AI-based modeling and optimization of RF/microwave components.

Tutorial

Tutorial 02: Smart Sensing SoCs Based on Heterogeneous CMOS-MEMS Integration and Sensor-AI Co-Designed Architectures

14:00-17:00, October 27, 2026 @Yaxu Hall

Tutorial Abstract

Smart sensing system-on-chips (SoCs) are becoming a critical hardware foundation for edge intelligence, secure perception, Internet of Things, healthcare monitoring, aerospace systems, and industrial sensing. As sensing terminals move closer to the physical world, they are expected not only to acquire signals, but also to extract features, perform intelligent recognition, support secure authentication, and make energy-efficient decisions. This trend is driving the evolution from conventional sensor chips toward highly integrated smart sensing SoCs that combine advanced sensing front ends, low-noise circuits, embedded computing, AI acceleration, heterogeneous integration, and hardware security. This tutorial will present recent advances in smart sensing SoCs from two complementary perspectives: sensor-AI co-designed image sensing architectures and heterogeneous CMOS-MEMS integrated sensing systems. The first part focuses on intelligent CMOS image sensing SoCs integrating in-sensor computing, event-driven acquisition, edge-AI processing, and hardware-level security. The second part discusses CMOS-MEMS sensing SoCs, emphasizing MEMS-ASIC co-design, post-CMOS fabrication, thermal sensing principles, cross-domain noise optimization, and practical applications.

The tutorial will first introduce image sensing SoCs inspired by biological vision. Dynamic vision sensors, also known as event-based vision sensors, have attracted increasing attention due to their sparse data representation, high temporal resolution, low latency, wide dynamic range, and high energy efficiency. Unlike conventional frame-based sensors, DVS pixels generate asynchronous events only when local intensity changes occur, reducing redundant data transmission and computation. However, existing DVS chips often discard static spatial information that is also important for robust visual recognition and decision-making. To address this limitation, a global-shutter-based dual-mode hybrid image sensing SoC with in-pixel adaptive conversion gain will be presented. This architecture combines active pixel sensor imaging and dynamic vision sensing to acquire both static and dynamic scene information efficiently. The tutorial will further discuss end-to-end sensor-AI co-design. In conventional edge vision systems, CMOS image sensors and AI processors are often designed separately, causing excessive data movement, interface overhead, and algorithm-hardware mismatch. A representative image sensing SoC with an integrated highly energy-efficient edge convolutional neural network processor will be introduced, highlighting joint optimization of the sensing front end, data representation, neural network model, and hardware accelerator. In addition, hardware-level security for trustworthy imaging will be addressed through an in-sensor hardware security architecture based on an optically reconfigurable physical unclonable function, which provides a sensor-level root of trust against emerging spoofing and synthetic-content attacks.

The second part of this tutorial will focus on heterogeneous CMOS-MEMS integrated sensing SoCs. MEMS, or micro-electromechanical systems, enables sensors with miniaturized form factors, low power consumption, and high sensitivity. When integrated with CMOS technology, these sensors can further benefit from compact system architecture, reduced parasitic effects, improved signal integrity, and high

signal-to-noise ratio. However, the development of high-performance CMOS-MEMS sensing SoCs still faces several key challenges, including MEMS-ASIC co-design, thermal isolation, CMOS-compatible post-processing, and cross-domain noise optimization. In this tutorial, a system-level modeling framework for the cooperative design of CMOS-MEMS thermal flow sensing SoCs will first be introduced. Post-CMOS processing strategies for MEMS structure thinning, thermal isolation enhancement, and sensor performance improvement will then be discussed. Representative thermal flow, acceleration, and pressure sensing SoCs will be presented, with emphasis on jointly analyzing and optimizing mechanical-domain and electrical-domain noise to improve signal-to-noise ratio and limit of detection. Finally, application examples in smart building airflow monitoring, respiration sensing, and IC thermal characterization will be introduced.

Overall, this tutorial will provide attendees with a comprehensive view of smart sensing SoCs by bridging system-level sensor design, sensor-AI co-design, hardware security, heterogeneous CMOS-MEMS integration, and practical sensing applications.

Tutorial Speaker(s)



Xiaojin Zhao
Shenzhen University, China

Talk Title: Smart and Secure CMOS Image Sensing SoCs Featuring Sensor-AI and Sensor-PUF Co-Designed Architectures

Bio.: Xiaojin Zhao is a Distinguished Professor of Shenzhen University, affiliated with the State Key Laboratory of Radio Frequency Heterogeneous Integration. He received dual B.Sc. degrees in microelectronics and applied mathematics from Peking University in 2005, and his Ph.D. in electrical and electronic engineering from the Hong Kong University of Science and Technology (HKUST) in 2010. He was a Postdoctoral Research Associate at HKUST and a Visiting Scholar at IMEC, Belgium. His research focuses on CMOS/MEMS monolithic image sensors, gas sensors, and trustworthy sensing technologies based on PUFs and TRNGs. He has published 120 international journal and conference papers. He is an IEEE Senior Member, Associate Editor of IEEE Sensors Journal, and technical committee member of IEEE CASS. He has served as the Vice Chair and the Chair for the IEEE EDSSC Shenzhen Joint Chapter (2015-2019), and also served as the Chair for the IEEE CAS Shenzhen Chapter (2020-2023).



Wei Xu
Shenzhen University, China

Talk Title: Smart Flow Sensing SoCs based on Monolithic Integration and MEMS-IC Co-design

Bio.: Wei Xu is a Tenured Associate Professor, Distinguished Research Fellow, and Ph.D. Supervisor. He is a recipient of the Guangdong Provincial Excellent Young Scientist Award and Shenzhen Overseas High-Level Talent, a Senior Member of IEEE, a member of the IEEE CASS Sensor Systems Technical Committee, an Associate Editor of IEEE Sensors Journal, and a Visiting Scholar at BSAC, UC Berkeley in 2024. He received his B.Eng. and M.Eng. degrees from Huazhong University of Science and Technology in 2010 and 2013, and his Ph.D. from Hong Kong University of Science and Technology in 2017. His research focuses on CMOS-MEMS sensing chips and microsystem integration. He has developed over ten high-performance sensing chips, published 80 SCI/EI papers, received the IEEE MEMS 2020 Best Paper Award, filed 11 Chinese patents, and led 15 research projects.

Tutorial

Tutorial 03: Breaking the AI-Computing Driven Interconnect Bottleneck

16:00-17:30, October 27, 2026 @Yuqing Hall

Tutorial Abstract

The explosive growth of generative AI and large language models (LLMs) has created an unprecedented compute-interconnect co-design challenge. As AI accelerators scale to tens of thousands of chips per cluster, data movement has surpassed computation as the dominant consumer of power and the primary limiter of system performance. This tutorial addresses the critical interconnect technologies that enable next-generation AI computing: the scaling of serial links toward 224Gbps per lane and advanced crosstalk cancellation techniques for high-density parallel interfaces. We will present fundamental physical limits, state-of-the-art circuit architectures, and emerging solutions from leading industry and academic groups. Special emphasis will be placed on how interconnect design is evolving to meet the unique requirements of AI computing workloads, including low latency, high energy efficiency, and massive bandwidth density. Attendees will gain deep insights into the cross-layer design tradeoffs spanning circuits, packaging, and system architecture that are shaping the future of computing systems. This tutorial is intended for circuit designers, system architects, and researchers working in high-speed communication, VLSI design, and AI hardware acceleration.

Tutorial Speaker(s)



Yuan Du
Nanjing University, China

Talk Title: High-speed Parallel Interconnects: Crosstalk Cancellation Techniques

Bio.: Yuan Du received B.S. degree with honor from Southeast University (SEU), and Ph.D. degree both from University of California, Los Angeles (UCLA). Since 2019, he has been with Nanjing University, Nanjing, China, as an Associate Professor. His current research interests include designs of high-speed inter-chip/intra-chip interconnect circuits, RFICs, and machine-learning hardware accelerators. He was the recipient of the Microsoft Research Asia Young Fellow (2008), Southeast University Chancellor's Award (2009), Broadcom Fellow (2015), and IEEE Circuits and Systems Society Darlington Best Paper Award (2021).

Tutorial

Tutorial 04: Artificial Intelligence for 6G: Implementations, Algorithms, and Optimizations

14:00-15:30, October 27, 2026 @Yuqing Hall

Tutorial Abstract

This tutorial focuses on the very popular topic "Artificial Intelligence for 6G: Circuits, Systems, and Optimizations". Due to its undoubted significance, research combining "AI" and "6G" has drawn lots of attentions from both academia and industry. Although some initiatives related to "AI for 6G" have been named, their design, implementation, and optimization are unfortunately not complete and of course in infancy. Having lots of potential for AI's new innovations, advances are required in network architectures, signal processing solutions, semiconductor technologies as well as in its optimization regarding the overall wireless system design. Much of the research has scattered on the design, implementation, and optimization of the corresponding circuits and systems. This tutorial would like to emphasize its uniqueness on "AI for 5G and B5G" related VLSI/IC designs and help audience to know the cutting-edge progresses from the perspective of circuits and systems. With a focus on bridging the gaps between theory and practical implementations, the goal of this tutorial is to demonstrate the latest research progress on circuits and systems design for efficiently realizing machine learning in wireless communications. The tutorial will bring together academic and industrial aspects to identify technical challenges and recent results related to this area, including Big Data Processing, Artificial Intelligence, Internet of Things, 6G, and Multi-Gigabit Optoelectronics Communications.

Tutorial Speaker(s)



Chuan Zhang

Southeast University, China; Purple Mountain Laboratories, China

Talk Title: Artificial Intelligence for 6G: Implementations, Algorithms, and Optimizations

Bio.: Chuan Zhang received the B.E. degree in microelectronics and the M.E. degree in very-large scale integration (VLSI) design from Nanjing University, Nanjing, China, in 2006 and 2009, respectively, and the Ph.D. degree from the Department of Electrical and Computer Engineering, University of Minnesota, Twin Cities (UMN), USA, in 2012.

He is currently the Young Chair Professor of Southeast University. He is also with the LEADS, National Mobile Communications Research Laboratory, Frontiers Science Center for Mobile Information Communications and Security of MoE, Quantum Information Center of Southeast University, and the Purple Mountain Laboratories, Nanjing, China. His current research interests are algorithms and implementations for signal processing and communication systems.

Dr. Zhang served as an Associate Editor for the IEEE Transactions on Signal Processing, IEEE Transactions on Circuits and Systems - II, and IEEE Open Journal of Circuits and Systems, and a Corresponding Guest Editor for the JETCAS three times. He served as a Senior Editorial Board (SEB) member for the IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), and a Steering Committee member for the IEEE Transactions on Mobile Computing. He was a Distinguished Lecturer and the Chair of the Circuits and Systems for Communications TC of the IEEE Circuits and Systems Society. He is also a member of the Applied Signal Processing Systems TC of the IEEE Signal Processing Society, and Circuits and Systems for

Communications TC, VLSI Systems and Applications TC, and Digital Signal Processing TC of the IEEE Circuits and Systems Society. He received the Best Contribution Award of the IEEE Asia Pacific Conference on Circuits and Systems (APCCAS) in 2018, the Best Paper Award in 2016, the Best (Student) Paper Award of the IEEE International Conference on DSP in 2016, three Best (Student) Paper Awards of the IEEE International Conference on ASIC in 2015, 2017, 2019, and 2023, the Best Paper Award Nomination of the IEEE Workshop on Signal Processing Systems in 2015, three Excellent Paper Awards and two Excellent Poster Presentation Awards of the International Collaboration Symposium on Information Production and Systems from 2016 to 2018, the Outstanding Achievement Award of the Intel Collaborative Research Institute in 2018, and the Merit (Student) Paper Award of the IEEE APCCAS in 2008. He also received the Three-Year University-Wide Graduate School Fellowship of UMN and the Doctoral Dissertation Fellowship of UMN.

Tutorial

Tutorial 05: Advanced Memory Systems: Reliable Storage and Efficient Computing

14:00-17:00, October 27, 2026 @Huanying Hall

Tutorial Abstract

Advanced memory systems play a critical role in the AI era, as growing data volumes and computational demands place increasing pressure on storage and processing capabilities. Ensuring reliable data storage and supporting energy-efficient computing are two key directions in their development. The first talk addresses error correction codes for next-generation NAND flash memory. It begins with an overview of NAND flash reliability challenges and error correction fundamentals, then introduces two-dimensional turbo product codes. Implementation and evaluation considerations are discussed to highlight practical design trade-offs, followed by a summary and outlook on future developments in NAND flash error correction. The second talk examines computing-in-memory (CIM) readout circuit design and optimization. It explains how analog accumulation and output quantization affect accuracy, throughput, energy consumption, and area efficiency. Representative techniques and circuit examples illustrate performance trade-offs in different CIM readout architectures, emphasizing the co-design of accumulation and quantization to reduce conversion overhead while meeting computational requirements. This tutorial is intended for researchers and engineers working in memory technologies, integrated circuit design, and AI hardware.

Tutorial Speaker(s)



Jianjun Luo
Hangzhou Dianzi University, China

Talk Title: Error Correction Codes for Next-Generation NAND Flash Memory

Bio.: Jianjun (Jerome) Luo, the Dean of Microelectronic Research Institute in Hangzhou Dianzi University, also the founder and CTO of Sage Microelectronics. He earned a PhD in semiconductor technology from Zhejiang University in China, a Master's in Microelectronics from the Hangzhou Dianzi University, and a Bachelor's in Electronics Engineering from Shanghai Jiao Tong University. He accumulated his experience in communication and storage IC design for more than 30 years. He won the second prize of National Scientific and Technological Progress Award, and Ho Leung Ho Lee Foundation's Scientific and Technological Award.



Wei Mao
Xidian University, China

Talk Title: Computing-in-Memory Readout Circuits: Design Principles and Optimization

Bio.: Wei Mao received the B.Eng. degree from Southeast University and the Ph.D. degree from the National University of Singapore. Since 2023, he has been an Associate Professor with Xidian University, Xi'an, China. His research interests include emerging computing and memory chip design for AI

applications. He has published over 90 papers in leading journals and conferences, along with one first-author monograph and two book chapters. His awards include the Second Prize of the 2020 Wu Wenjun Artificial Intelligence Chip Award, the 2021 Ministry of Education-Huawei "Intelligent Foundation" Pioneer Teacher Award, and the Best Live Demonstration Award at IEEE AICAS 2026. He serves on the IEEE Circuits and Systems Society Standards Committee and the executive committees of CCF's Integrated Circuit Design and Information Storage Technology Technical Committees. He is an Associate Editor of ICAS and a Guest Editor of IEEE TCAS-I. He has also served on the organizing or technical program committees of conferences including ISCAS, ISICAS, and AICAS.

Competition Session

Analog Competition Topic: AI Agent-Based Automatic Optimization Design of FVF LDO

Time	14:00-15:30, October 27, 2026	Venue	Shuibo Hall
Session Chair	Cangyuan Li, Institute of Computing Technology, CAS, China		

Session Details	
1186	**AI-Agent-Driven Automated Design Optimization of FVF LDOs: A Parameterized Framework** **Yiyu Chen, Jing Wang*, Jiafei Yao*, Jingyu Gu, Yi Kang, Yufeng Guo** Nanjing University of Posts and Telecommunications, China
4439	**Automated FVF-LDO Sizing via Simulation-in-the-Loop Reinforcement Learning with LLM-Assisted Configuration** **Ruizheng Li[1,†], Han Wu[1,2,†], Qihang Chen[1], Binxin Huang[1], Lanhaoyue Wang[1], and Junmin Jiang[1,*]** [1]Southern University of Science and Technology, China [2]University of Macau, China

Sponsor

Shenzhen Lixin Semiconductor Co., Ltd.

Founded in 2018, Honedchip Semiconductor, is a National High-tech Enterprise and a Specialized and Innovative SME. The company specializes in ASIC chip solutions and focuses on cost-effective consumer-grade chips, high-performance power supplies, motor control, industrial and automotive-grade chips and other fields. Headquartered in Shenzhen, the company has chip design teams in Shanghai, Dalian, Chengdu, Chongqing, Xi'an and other cities. Since its establishment, it has continuously gained recognition from the capital market and entered a new stage of larger-scale development. Its technical team has filed a total of 126 intellectual property rights applications, including 46 invention patents, and has participated in the revision of 3 national standards.

Competition Session

Digital Competition Topic: AI Agent-Based NPU Design and Verification

Time	15:30-17:00, October 27, 2026	Venue	Shuibo Hall
Session Chair	Cangyuan Li, Institute of Computing Technology, CAS, China		

Session Details	
1756	**An Integer-First FastViT-T8 NPU: Technical Route and SKY130 Evaluation** **Chen Chen[1], Yu Hao[1], Letian Huang[1], Chaoyue Zheng[1]** [1]University of Electronic Science and Technology of China, China
6194	**Agent-Guided Design and Verification of a FastViT-T8 NPU in SKY130** **Rui Jiang[1], Shengyang Zhao[1], Ying Lu[1], Letian Huang*[1]** [1] University of Electronic Science and Technology of China, China
8544	**Reparameterization-Aware FastViT-T8 NPU: An Agent-Assisted Preliminary Design** **Shubham Kumar** Independent Researcher, IIT Kanpur graduate

Sponsor

Shanghai UniVista Industrial Software Group Co., Ltd.

Shanghai UniVista Industrial Software Group Co., Ltd. ("UniVista") is an EDA, IP and design solutions provider committed to serving semiconductor companies worldwide. We aim to become a trusted partner that achieves continuous market success through technology innovation.

Outstanding Young Scholar Award Session

Time	15:45-18:15, October 28, 2026	Venue	Guofeng Hall I
Session Chair	Cheng Zhuo, Zhejiang University, China		

Order	Details
01	**Xuan Li** University of Electronic Science and Technology of China, China
02	**Junmin Jiang** Southern University of Science and Technology, China
03	**Jiafei Yao** Nanjing University of Posts and Telecommunications, China
04	**Bobo Tian** East China Normal University, China
05	**Zhou Jin** Zhejiang University, China
06	**Jian Pang** Shanghai Jiao Tong University, China

Special Session

Special Session 1: Ferroelectric Materials and Devices-I

Time	13:30-15:30, October 28, 2026	Venue	Guofeng Hall I
Session Chair	Xiao Yu, Xidian University, China		

Session Details		
13:30	Keynote	**Hafnia-based Ferroelectric Devices for Memories and AI Applications** **Qianqian Huang** Peking University, China
14:00	Invited	**A New Perspective on the Classification of Inorganic Ferroelectrics** **Kanhao Xue** Huazhong University of Science and Technology, China
14:20	Invited	**Ultrawide MW Hf-based FeFET Technology and Its Application in Reconfigurable Digital-analog Architectures** **Ran Cheng** Zhejiang University, China
14:40	Invited	**Reliability Degradation Mechanisms and Ultrathin Processing of HfO2-Based Ferroelectric Films** **Jixuan Wu** Shandong University, China
15:00	1816	**Revealing the Mechanism of Sacrificial Layer Engineering in Si-Channel MIFIS FeFETs for Enhanced Device Performance** **Yuliang Ji[1,2,3], Ruoyao Ji[1,2,3], Zeqi Chen[2,3], Yajing Ding[2,3], Min Liao[2,3], Xiaoyu Ke*[2,3], Junshuai Chai[2,3],Hao Xu[2,3], Xiaolei Wang[2,3], Wenwu Wang[2,3] and Tianchun Ye[2,3]** [1] University of Chinese Academy of Sciences, China; [2] Chinese Academy of Sciences, China; [3]Chinese Academy of Sciences, China
15:15	6560	**Coupled Al2O3 Interlayer and HZO Ferroelectric Layer Engineering for Memory Window-Operation Voltage-Retention Optimization in FeNAND** **Jia Yang[1,2,3], Runhao Han[2,3], Yajing Ding[2,3], Wenbo Fan[1,2,3], Zeqi Chen[2,3], Ruoyao Ji[1,2,3], Xianzhou Shao*[2,3], Hao Xu[2,3], Xiaolei Wang[2,3]** [1]University of Chinese Academy of Sciences, China; [2]Chinese Academy of Sciences, China; [3]Chinese Academy of Sciences, China

Special Session

Special Session 1: Ferroelectric Materials and Devices-II

Time	13:30-15:30, October 29, 2026	Venue	Guofeng Hall I
Session Chair	Xiuyan Li, Shanghai Jiao Tong University, China		

Session Details		
13:30	Keynote	**Hafnium based ferroelectric si channel NAND FlashHafnium based ferroelectric Si channel NAND Flash** **Xiaolei Wang** Chinese Academy of Sciences, China
14:00	Invited	**Giant Tunneling Electroresistance in Sliding Ferroelectrics** **Jiangbin Wu** Chinese Academy of Sciences, China
14:20	Invited	**Alternating Atomic-dipole Layers and Switching Dynamics in Al1-xScxN Ferroelectrics** **Yan Cheng** East China Normal University, China
14:40	Invited	**3D-Stackable Ferroelectric Computing-in-Memory for LLMs** **Jin Luo** Beihang University, China
15:00	6374	**Improved Retention and Read Disturb Immunity in Hf0.5Zr0.5O2-Based FeFET Enabled by an Al2O3/La2O3 Bilayer Gate Interlayer** **Ruoyao Ji[1,2], Zeqi Chen[1,3], Tao Hu[1,3], Yuhan Li[1,3], Junshuai Chai*[1,3], Hao Xu[1,3], Xiaolei Wang[1,3], Wenwu Wang[1,3] and Tianchun Ye[1,3]** [1]Chinese Academy of Sciences, China; [2]University of Chinese Academy of Sciences, China; [3]University of Chinese Academy of Sciences, China
15:15	6399	**Antiferroelectric Zr-Doped HfO2 Blocking Layer for Charge-Trapping Flash with a 9.22-V Memory Window and Reduced Operation Voltage** **Kaiyi Li[1,2,3], Yuanyuan Zhao[1,3], Mingkai Bai[1,3], Xinpei Jia[1,3,*], Tao Hu[1,3], Yajing Ding[1,3], Ruoyao Ji[1,3], Haofeng Wang[1,3], Mengjie Zhao[1,3], Xiaoqing Sun[1,3], Junshuai Chai[1,3], Hao Xu[1,3], Xiaolei Wang[1,3]** [1]Chinese Academy of Sciences, China; [2]University of Chinese Academy of Sciences, China; [3]University of Chinese Academy of Sciences, China

Special Session

Special Session 1: Ferroelectric Materials and Devices-III

Time	16:00-18:00, October 29, 2026	Venue	Guofeng Hall I
Session Chair	Jin Luo, Beihang University, China		

Session Details		
16:00	Keynote	**Toward Large-Scale Hafnia-Based Ferroelectric Memory: From Device Optimization to Megabit-Scale Memory Macro** **Hangbing Lv** Xiamen University, China
16:30	Invited	**Modeling the Polarization Dynamics and Reliability Failure in HfO2-Based Ferroelectrics** **Bing Chen** Xidian University, China
16:50	Invited	**Thermal and Electrical Filed Induced Phase Transition in Ferroelectric HfxZr1-xO2 Thin Films** **Xiuyan Li** Shanghai Jiao Tong University, China
17:10	Invited	**Simulation Study of TDDB Characteristics in HfO_2 ferroelectric Dielectrics Based on the TCAD Kinetic Monte Carlo Method** **Fei Mo** Beijing Institute of Technology, China
17:30	1783	**Edge-mediated Oxygen Degradation Governs the Thermal Reliability of Wurtzite Ferroelectric AlScN** **Ruiqing Wang[1], Siying Zheng[1, 2]*, Wenxin Sun[1], Zhe Chen[2], Xinghui Wang[1], Xihui Yuan[1, 2], Feng Zhu[2], Haiwen Xu[1, 2], Bochang Li[1, 2], Tao Wu[3], Bing Chen[1, 2], Jiuren Zhou[1,2]*, Yan Liu[1, 2], Yue Hao[1, 2], and Genquan Han[1, 2]** [1]Xidian University, China; [2]Hangzhou Institute of Technology, Xidian University, China; [3]ShanghaiTech University, China
17:45	4569	**Experimental Dataset–Driven AI Design for HfxZr1-xO_2 Ferroelectric Devices** **Xinrui Ma[1†], Danyang Chen[1†], Zhiyu Lin[1], Mengwei Si[1], Dongdong Li[2], Xiuyan Li[1]*** [1]Shanghai Jiao Tong University, China; [2] Zhangjiang Laboratory, China

Special Session

Special Session 1: Ferroelectric Materials and Devices-IV

Time	09:00-10:20, October 30, 2026	Venue	Guofeng Hall I
Session Chair	Zhiyuan Fu, Southeast University, China		

Session Details		
09:00	Invited	**Defect and Reliability Physics: from Si to Emerging Devices** **Yue-Yang Liu** Chinese Academy of Sciences, China
09:20	Invited	**HZO-Based Oxide-Semiconductor FeFETs for Dynamic Information Processing** **Sungjun Kim** Dongguk University, Korea
09:40	Invited	**Ferroelectric Memory for Power-Efficient and Reliable Computing-in-Memory** **Xiwen Liu** The Hong Kong University of Science and Technology (Guangzhou), China
10:00	Invited	**Ultralow Fatigue in Hafnia-based Ferroelectric Capacitor Achieved Through Regulation of Oxygen Vacancy Distribution** **Xubing Lu** South China Normal University, China

Special Session

Special Session 1: Ferroelectric Materials and Devices-V

Time	10:45-12:00, October 30, 2026	Venue	Guofeng Hall I
Session Chair	Xiwen Liu, The Hong Kong University of Science and Technology (Guangzhou), China		

Session Details		
10:45	Invited	**Low Defect Density FFerroelectric Semiconductors and High-k Dielectrics** **Yu Zhou** Central South University, China
11:05	Invited	**CMOS-Compatible 3D Hafnium-Based Ferroelectric Materials, Devices, and Memory Chips** **Lin Chen** Fudan University, China
11:25	Invited	**Ferroelectric Compute-in-Memory Annealer for Combinatorial Optimization** **Xunzhao Yin** Zhejiang University, China
11:45	9727	**Total Ionizing Dose Effects on HfO2-Based 3D Trench Ferroelectric Capacitors** **Zheng Zhang[1], Huan Liu*[1,2], Yulin Zhang[1], Peiyuan Du[1], Fei Yu[1,2], Yong Wang[1], Xiao Yu[1,2], Yan Liu[1], Yue Hao[1], Genquan Han[1,2]** [1]Xidian University, China; [2]Hangzhou Institute of Technology, Xidian University, China

Special Session

Special Session 1: Ferroelectric Materials and Devices-VI

Time	13:30-15:20, October 30, 2026	Venue	Guofeng Hall I
Session Chair	Xiao Yu, Xidian University, China		

Session Details		
13:30	Invited	**From Polarization Decoupling to Defect Dynamics: Rethinking Imprint and Fatigue in HfO_2-Based Ferroelectrics** **Lang Zeng** Beihang University, China
13:50	Invited	**Hafnium-Based Ferroelectrics: From Polarization Mechanisms to Advanced Device Applications** **Houfang Liu** Tsinghua University, China
14:10	Invited	**Hafnia-Based Fusion FeRAM for High-Speed Edge LLM Applications** **Zhiyuan Fu** Southeast University, China
14:30	Invited	**Ultrahigh Endurance in Wurtzite Ferroelectrics through Nitrogen-Vacancy Confinement** **Haiwen Xu** Xidian University, China
14:50	4638	**Thermal Stress Simulation and Comparative Analysis in 2D/3D HZO-Based Capacitors** **Hejianhui Wang[1], Yunfei Sun[2], Mengwei Si[1,*], Wei Tang[1,*], Dongdong Li[2,*]** [1]Shanghai Jiao Tong University, China; [2] Zhangjiang Laboratory, China
15:05	1943	**Universal Analytical Modeling of 3D Cylindrical FeCAPs: Screening Radius and Tolerance to Structural Defects** **Xiang Li, Shujun Gao, Xinyue Feng, Hengxi Liu, Renjie Zheng, Hailong You, Cong Li*** Xidian University, China

Special Session

Special Session 2: Oxide Semiconductor Devices-I

Time	13:30-15:15, October 28, 2026	Venue	Qinglian Hall
Session Chair	Sunbin Deng, Huazhong University of Science and Technology, China		

Session Details		
13:30	Keynote	**Oxide Semiconductors for Future DRAM: Materials, Devices, and 3D Integration** **Guilei Wang** Beijing Superstring Academy of Memory Technology, China
14:00	Invited	**A Multimodal Optoelectronic Reservoir Computing System Based on ZnO Thin-film Transistors** **Yuanyuan Shi** University of Science and Technology of China, China
14:20	Invited	**High-Performance p-Channel Tellurium-based Oxides TFTs and CMOS Circuits** **Ao Liu** University of Electronic Science and Technology of China, China
14:40	Invited	**Probing Disorder-Induced Localized Electronic States in Low-Dimensional Oxide Semiconductors** **Chang Niu** National University of Singapore, Singapore
15:00	1238	**Non-Unique Trap Density of States Extraction in IGZO Thin Film Transistors Using TCAD-Assisted Machine Learning** **Hequn Zhou, Liankai Zheng, Mengwei Si*** Shanghai Jiao Tong University, China

Special Session

Special Session 2: Oxide Semiconductor Devices-II

Time	13:30-15:35, October 29, 2026	Venue	Qinglian Hall
Session Chair	Mengwei Si, Shanghai Jiao Tong University, China		

Session Details		
13:30	Keynote	**Integrating Oxide Thin-film Transistors for Opto-electric Applications** **Chuan Liu** Sun Yat-sen University, China
14:00	Invited	**Simulation Study of Complementary Ferroelectric FET (CFeFET) for Reliable Multibit Content Addressable Memory** **Fei Mo** Beijing Institute of Technology, China
14:20	Invited	**Metal-Oxide Thin-Film Transistors for Flexible Power Electronics: From High-Voltage Devices to Integrated Power Management Circuits** **Wangran Wu** Southeast University, China
14:40	Invited	**Recent Developments in IGZO 2T0C DRAM Technology** **Guanhua Yang** Chinese Academy of Sciences, China
15:00	Invited	**BEOL-compatible Devices and its 3D Integration Technology** **Yuye Kang** Huazhong University of Science and Technology, China
15:20	9149	**Oxygen-Partial-Pressure-Controlled ZSO Passivation for Highly Stable ITZO TFTs** **Junquan Lin[1], Xiaocheng Wang[1], Rongsheng Chen*[1]** [1]South China University of Technology, China

Special Session

Special Session 3: Advanced Memory and Computing-In-Memory Circuit Design

Time	09:00-10:00, October 30, 2026	Venue	Shuibo Hall
Session Chair	Chaoyue Zheng, Yangtze Delta Region Institute (Huzhou), University of Electronic Science and Technology of China, Huzhou, China		

Session Details		
09:00	5732	**A Hybrid-Domain SRAM-CIM MAC Architecture with High-Parallelism and Shared Quantization** **Jinnan Wu[1], Xianluan Zhao[3], Zhengjun Ye[1], Chang Liu[1], Yue Zhao*[1,2], Shibin Lu[1], Changyong Liu[1]** [1]Hefei Normal University, China; [2]Yangtze Delta Region Institute (Huzhou), University of Electronic Science and Technology of China, China; [3]Anhui University, China
09:15	8284	**Execution-Semantics-Aware Boundary Architecture for RRAM-CIM/Digital Heterogeneous Systems** **Yuankun Li[1], Qingtian Zhang[1], Bin Gao[1,2], Huaqiang Wu[1,2]** [1]Tsinghua University, China; [2]Beijing National Research Center for Information Science and Technology (BNRist), China
09:30	8579	**Research on Optimization Methods of Test Vector Compression Based on MS8000 ATE Tester** **Yu An[1], Wenkai Du[2], Chaoyue Zheng[2], Letian Huang[2], Donghuang Wang*[1]** [1] Huzhou Normal University, China; [2] Yangtze Delta Region Institute (Huzhou), University of Electronic Science and Technology of China, China
09:45	0729	**Design and Analysis of a MOS-Based Floating Memristor Emulator** **Jiajun Huang[1,2], Zerong Lan[1,2], Ziheng Fu[1,2], Chunlin Ji[3], Jingjing Liu*[1,2]** [1]Sun Yat-sen University, China; [2]Guangdong Provincial Key Laboratory of Sea-Air-Space Communication, China; [3]Kuang-Chi Institute of Advanced Technology, China

Technical Session

Technical Session 01: General Analog-I

Time	13:30-15:25, October 28, 2026	Venue	Huanying Hall
Session Chair	Yang Liu, Xidian University, China		

Session Details		
13:30	Invited	**Active Gate Driver Chips for Power Switches** **Run Min** Huazhong University of Science and Technology, China
13:50	Invited	**High-Precision Voltage and Frequency Reference Circuits** **Zhuojun Chen** Hunan University, China
14:10	5164	**A Biosignal Acquisition AFE with 15.38 GΩ Input Impedance and 64 VPP Common-Mode Interference Cancellation Range** **Yinuo Zhang[1], Chenghao Zhou[1], Xiangyi Liu[1], Jie Yin[1], Zixuan He[1], Xufeng Liao[1,2] and Lianxi Liu*[1,2]** [1]Xidian University, China; [2]Xidian University Chongqing ICs Innovation Institute, China
14:25	2772	**Coarse/Fine-Decoupled Group-Predictive Calibration for Partially Interleaved Pipelined-SAR ADCs** **Chuanbin Gong[1], Haoyu Sheng[1], Ruizhe Zhang[1], Chao Luo*[1]** [1]University of Science and Technology of China, China
14:40	3610	**A Low-OSR 3rd-Order EF-CIFF Noise-Shaping SAR ADC With an Offset-Cancelled Shared Amplifier** **Yi Wang[1], Yunbei Si[1], Hui Zhou[1], Guanghan Zhang[1], and Shuang Xie[1*]** [1]Shandong University, China
14:55	2565	**A 22.9 mW Double-Sampling Supply Compressed Zoom SDM with 108 dB SNDR in 128 kHz BW** **Xu Liu[1], Pengcheng Wang[1], Jun Meng[2], Tao Liu[2], Zhaohao Wang*, Hui Zhang*** [1]Beihang University, China; [2]Nanjing Micro One Electronics Inc. Nanjing, China
15:10	3372	**A 12-Bit Current-Steering DAC With a Randomized Pointer Direction DWA Method** **Chengjie Huang[1,2], Shuyan Zhu*[1,2], Shaolin Liao[3], Yunchu Li[1,2]** [1]Sun Yat-sen University, China; [2] Zhuhai Key Laboratory of Millimeter-wave Terahertz Antenna and RFIC, SYSU, Zhuhai, China; [3]Sun Yat-sen University, China

Technical Session 02: Power Devices & Power IC-I

Time	13:30-15:10, October 28, 2026	Venue	Yuqing Hall
Session Chair	Qimeng Jiang, Southwest Jiaotong University, China		

Session Details		
13:30	Invited	**Total-Ionizing-Dose Effect in SOI LDMOS: New Insight and New Radiation Hardening Strategy** **Xin Zhou** University of Electronic Science and Technology of China, China
13:50	Invited	**Monolithic Integration of E/D-Mode GaN HEMTs Based on p-NiO Gates** **Denggui Wang** Nanjing Electronic Devices Institute, China
14:10	9452	**A 4H-SiC VDMOS With Embedded Channel Resembling JFET to Enhance Short-Circuit Withstand Capability** **Yiru He[1], Xinwei Song[2], Hang Chen[2], Bo Zhang[1], Yourun Zhang*[1,3]** [1]University of Electronic Science and Technology of China, China; [2] China Zhenhua Group Yongguang Electronics Co., Ltd., China; [3]University of Electronic Science and Technology of China, China
14:25	9183	**A Novel Unipolar-Bipolar Hybrid-Mode SOI-LIGBT With Homogenization Field Plate** **Rongshuo Liu[1], Teng Liu[1,2], Yongshun Li[1,2], Yiduo Xie[1], longhui Lin[1], Zhenyan Liu[1], Yueyu Zhang[1], Shengyuan Wang[1], Zhili Zhang[2], Hua Song[2], Shixiong Chong[2], Nailong He[2], Sen Zhang[2], Yongsheng Sun[3], Hao Fang[3], Wentong Zhang[1*], Zhaoji Li[1] and Bo Zhang[1]** [1]University of Electronic Science and Technology of China, China; [2] CSMC Technologies Corporation, China; [3] Wuxi China Resources Microelectronics Co, China
14:40	7770	**Degradation Mechanism and Annealing Response of 1700V SiC MPS Diode Under Electron Irradiation** **Zhaoxu Song, Zheyuan Zhang, Suyu Xu, Yu Tian, Sheng Li, Ran Ye, Long Zhang*, Jiaxing Wei*,Siyang Liu, and Weifeng Sun** Southeast University, China
14:55	8272	**A Novel 3-D Split-Gate IGBT with Double-Gate Control for Reduced Turn-Off Loss** **Yige Zheng[1], Zehong Li*[1,2], Likun Zheng[1], Shuolei Jing[1], Yijie Zhao[1], Tongyang Wang[1], Ziming Xia[1], Zhaoqing Jin[1], Shuaibing He[1], Zhishuo Xu[1], Xuan Wang[1]** [1]University of Electronic Science and Technology of China, China; [2] Chongqing Institute of Microelectronics Industry Technology, University of Electronic Science and Technology of China (UESTC), Chongqing, China

Technical Session 03: RF & Wireless-I

Time	13:30-15:30, October 28, 2026	Venue	Huiyuan Hall
Session Chair	Zhaonian Yang, Xi'an University of Technology, China		

Session Details		
13:30	Keynote	**Noise-Cancelling Low-Noise Amplifier Design for 5G applications** **Zhe Liu** Tianjin University, China
14:00	Invited	**Radio Frequency Integrated Circuit Design for Satellite Communications** **Geliang Yang** Guangdong University of Technology, China
14:20	Invited	**On-Chip Terahertz Radiator and Phased Arrays** **Liang Gao** Southeast University, China
14:40	Invited	**Blocker-Tolerant Mixer-First Receivers for 5G-Advanced/6G FR3 Communications** **Kai Li** Tianjin University, China
15:00	5295	**A Sub-GHz Current-Reconfigurable MEMS Oscillator Core With Fast Start-Up and Low Steady-State Power** **Xijun Huang[1], Kai Tang[1,*], Li Ni[1], Ke Liu[1], Jingyu Hu[1], Yuchi Xiao[1], Keping Wang[2], Yuanjin Zheng[3]** [1]Hunan University, China; [2]Tianjin University, China; [3]Nanyang Technological University, Singapore
15:15	8809	**A 24.5–37.8-GHz 6-Bit Digitally-Controlled Variable Gain Amplifier with 24-dB-Range in 28nm CMOS** **Changxuan Wang, Sicheng Han, Yun Wang, Chen Jiang, Yun Yin and Hongtao Xu** Fudan University, China

Technical Session 04: Semiconductor Process Technologies-I

Time	13:30-15:05, October 28, 2026	Venue	Yaxu Hall
Session Chair	Ran Cheng, Zhejiang University, China		

Session Details		
13:30	Invited	**Amorphous IGZO Thin-Film Transistors on Unconventional and Flexible Substrates** **Niko Münzenrieder** Free University of Bozen, Italy
13:50	3321	**High-performance IGZO Thin-Film Transistors by Compensation Treatment** **Chuanlin Sun[1], Junchen Dong*[2], Xinru Shi[2], Dedong Han[1], Xing Zhang*[1]** [1]Peking University, China; [2]Beijing Information Science and Technology University, China
14:05	4143	**Direct Visualization of Plasma Doping for As and B by 1nm-resolution Scanning Spreading Resistance Microscopy: Conformal Doping Evaluation and Boron Dopant Fluctuation** **Li Zhang** Metrix Japan Corp., Japan
14:20	8349	**Investigation of Gate Work Function and ALD Oxidant Precursor on Performance of Metal/Al_2O_3/HfO_2/Al_2O_3/Si Charge Trapping Memory** **Longrong Huang[1,2], Yanyu Yang[1,2], Yupeng Lu[1,2], Gaobo Xu*[1,2], Huaxiang Yin*[1,2]** [1]Chinese Academy of Sciences, China; [2]University of Chinese Academy of Sciences, China
14:35	4140	**N2O Pre-Oxidation Enhanced 200-nm Vertical-Channel IGO Thin-Film Transistors with a Sidewall-Gate Architecture** **Jiahao Chen[1], Mengran Liu [1], Zhendong Jiang[1], Zhihao Lv[1], Shuheng Fu[1], Shengdong Zhang[1], Lei Lu*[1]and Xiaole Cui*[1]** [1]Peking University, China
14:50	9085	**STI Profile Control for SRAM Electrical Performance Enhancement: An Expertise-Embedded AI Approach in 40 nm CMOS** **Le Li[1#]*, XF Guan[1#]*, Rumeng Qiu[1], Tiantian Wang[1], Chih-Wei Lin[1], Chih-Peng Liang[1], Yi-Chuen Eng[1]*, Daiki Qin[1], Po-Ju Chen[1], Zhe-Ju Liu[1], Jhong-Sheng Wang[1], and Chia-Yen Li[1]** [1]Nexchip Semiconductor Corporation, China

Technical Session 05: Wireline

Time	13:30-15:20, October 28, 2026	Venue	Shuibo Hall
Session Chair	Bingyi Ye, East China Normal University, China Yuekang Guo, Shanghai Jiao Tong University, China		

Session Details

13:30	Invited	**Recent Research Progress on PAM4 Reference-less CDR** **Zhao Zhang** Chinese Academy of Sciences, China
13:50	2469	**A 12.5-Gb/s Clock and Data Recovery Achieving 0.51-UI Jitter Tolerance at 200-MHz with Stepped-Trajectory Phase Interpolator in 28 nm CMOS** **Xinran Huang, Wenlong Zhou, Yanke Chen, Chuangao Yan, Yintang Yang, Maliang Liu*** Xidian University, China
14:05	9655	**A 1.09pJ/bit 112Gb/s Wireline Receiver With 8-Way Time-Interleaved Track-and-Holds and Embedded Charge-Domain Equalization** **Chungen Lv[1], Huzhi Tang[1], Chao Yang[1], Yuekang Guo[1], Jing Jin[*1]** [1]Shanghai Jiao Tong University, China
14:20	8481	**A 28-Gbaud Tri-Mode SerDes Transmitter with Fractional-spaced Equalization and Hybrid Driver in 65 nm CMOS** **Shunhan Hu, Fangzhou Zhao, Zhuoli Huang, Chen Jiang*** Fudan University, Shanghai, China
14:35	6542	**A PVT-Adaptive 1-GS/s 8-bit SAR ADC Based on Comparator/CDAC Co-Reconfiguration** **Junle Wang[1,2], Xuan Guo*[1], Jiawei Ding[1,2], Hanbo Jia[1], Kai Sun[1], Ming Chen[1], Xinyu Liu[1]** [1]Chinese Academy of Sciences, China; [2]University of Chinese Academy of Sciences, China
14:50	7980	**A 12.5-Gb/s Inductorless Optical Receiver Analog Front End With Conjugate-Poles Based CTLE** **Qin Hu[1], Qi Mu[1], Yuhan Li[2], Ang Hu*[2], Dongsheng Liu[2],Xuecheng Zou[2]** [1]IEIT SYSTEMS Co., Ltd, China; [2]Huazhong University of Science and Technology, China
15:05	6837	**A Power-Efficient Resistive Feedforward Injection-Locked Ring VCO with Extended Frequency Tuning Range and Inherent Phase Calibration** **Jiechen Tian[1], Huzhi Tang[1], Yuekang Guo*[1], Jing Jin[1] and Jianjun Zhou[1]** [1]Shanghai Jiao Tong University, China

Technical Session 06: Digital Circuits-I

Time	13:30-15:00, October 28, 2026	Venue	Tianhan Hall
Session Chair	Junhui Wang, National University of Defense Technology, China		

Session Details		
13:30	9416	**3D DRAM-on-Logic Architecture for Long-Context Compressed LLM Inference Acceleration** **Jiawei Chen†, Yunhao Xiong†, Jiachen Chang, Liukai Xu, Yanan Sun*** Shanghai Jiao Tong University, China
14:00	8646	**A 28-nm 3T eDRAM-LUT CIM Macro with Sign-Bit-Dependent Accumulation for MXFP4/MXFP6 Low-Bit Floating-Point Inference** **Futao Li, Hao Wu, Kaijun Zhang, Jingyi Ma, Saifei Gou*, and Chixiao Chen*** Fudan University, China
14:15	0104	**RPCG: RRAM-Programmable Camouflaged Gate With Reference-Based Sensing** **Jiayi Yu[1,†], Li Ni[2,†], Xinrong Yang[1], Shimao Ren[1], Dameng Dai[1], Pengjun Wang[1,*]** [1]Wenzhou University, China; [2]Hunan University, China
14:30	6967	**SD-Tac: A Software–Hardware Co-Designed Spike-Driven Tactile Perception Method** **Chunlin Liu and Yi Kang*** University of Science and Technology of China, China
14:45	8390	**LoTeM-SER: Local Two-Stage Token Merging for Efficient Transformer-Based Speech Emotion Recognition** **Xiao Yan[1], Qi Cheng[1], Yupeng Gui[2], Sheng Zhou[2], Ruiqi Tang[2], Li Ding[1], Bingqian He[1], Shichen Peng[2], Han He[2], Qiuyu Li[2], and Yibo Fan[2,*]** [1]Xi'an University of Posts and Telecommunications, China; [2]Fudan University, China

Technical Session 07: Device Reliability & Security-I

Time	16:00-18:00, October 28, 2026	Venue	Qinglian Hall
Session Chair	Huaxing Jiang, South China University of Technology, China		

Session Details		
16:00	Keynote	**Application-Oriented Stability, Reliability, and Robustness of Wide-Bandgap Power Devices and ICs** **Yuhao Zhang** The University of Hong Kong, China
16:30	Invited	**Hot Carriers in Nanoscale FinFETs: From Degradation Mechanisms to Repair Strategies** **Hong Yang** Chinese Academy of Sciences, China
16:50	Invited	**Reliability of hafnium based ferroelectric Si channel NAND Flash** **Xiaolei Wang** Chinese Academy of Sciences, China
17:10	Invited	**β-Ga_2O_3 Vertical Trench MOSFETs with Quasi-Inversion Channel for Kilo-Volt Power Applications** **Xuanze Zhou** University of Science and Technology of China, China
17:30	5124	**Comparator-based Power Clamp Circuit for ESD and Surge Protections** **Zhaonian Yang*[1], Dongmu Tan[1], Leiming Zhu[1], Yuan Yang[1], Zhigang Ji[2]** [1]Xi'an University of Technology, China; [2]Shanghai Jiao Tong University, China
17:45	0003	**Temperature-Dependent Single-event Burnout Mechanism in P-GaN Gate HEMTs Under Heavylons Irradiation** **Jianggen Zhu[1], Shuting Huang[1], Fukang Yang[2], Jinggui Zhou[1], Xin Zhou[1], Danfeng Mao[4],Chao Feng[4], David Zhou[4], Bo Zhang[1] and Qi Zhou*[1,2,3]** [1]University of Electronic Science and Technology of China, China; [2] Shenzhen Institute for advanced study, UESTC, Shenzhen, China; [3] Institute of Electronic and Information Engineering in Dongguan, UESTC, Dongguan, China; [4] Shenzhen Pinghu Laboratory, Shenzhen, China

Technical Session 08: Design Methodology & EDA-I

Time	16:00-17:45, October 28, 2026	Venue	Huanying Hall
Session Chair	Ran Cheng, Zhejiang University, China		

Session Details		
16:00	9207	**BumpER: Fast yet Exact Through-Bump Current Computation for Early-Stage 3D PDNs** **Jingchao Hu*, Songyu Sun*, Qi Sun*, Zhou Jin*** *Zhejiang University, China
16:15	1220	**Reinforcement Learning-based Detailed Routing for Lithography Hotspot Reduction** **Zhanzi Chen[1, 2], Xiaohuan Ling[1], Yajuan Su*[1, 2], Xiaojing Su[1], Yuqin Wang[1], Pengyu Ren[1],Yujie Jiang[1], Tianao Chen[1], Fanqian Meng[1], Yayi Wei*[1, 2]** [1]Chinese Academy of Sciences, China; [2]University of Chinese Academy of Sciences, China
16:30	9487	**A Physics-Constrained Neural Compact Model for Ferroelectric Capacitors** **Hengxi Liu, Shujun Gao, Renjie Zheng, Wenyu Sun, Hailong You, Cong Li*** Xidian University, China
16:45	9296	**FORGE: A Hybrid LLM-Rule-Based Framework for Efficient Multi-Objective RRAM-IMC Design Space Exploration** **Yiman Gao[1], Lin Bao[1,*], Shuai Hu[2], Jingwei Sun[2], Haisu Zhang[2], Cuimei Wang[2], Ling Liang[2], Zheng Zhou[2], Zongwei Wang[2], Yimao Cai[2], Shanguo Huang[1]** [1]Beijing University of Posts and Telecommunications; [2] Peking University, China
17:00	0980	**Accelerating Device Iteration through AI-Driven Dual-Engine Framework** **Levi Chen[1]*, Wenhao Wu[1]*, Tiantian Wang[1], He Zhang, RR Zhu[1], Yi-Chuen Eng[1]*, Chih-Peng Liang[1], Daiki Qin[1], Po-Ju Chen[1], Shih-Ching Lee[1], Zhe-Ju Liu[1], Jhong-Sheng Wang[1], Chia-Yen Li[1], and Yibo Lin[2]** [1]Nexchip Semiconductor Corporation, China; [2]Peking University, China
17:15	5989	**A Closed-Loop AI Diagnosis-Optimization-Verification Flow for SRAM Design-Manufacturing Co-Optimization against Device Mismatch** **Leo Kuai[1#*], Yuri Ma[1#], Levi Chen[1], Chih-Wei Lin[1], Yi-Chuen Eng[1*], Po-Ju Chen[1], Chih-Peng Liang[1], Daiki Qin[1], Zhe-Ju Liu[1], Jhong-Sheng Wang[1], Chia-Yen Li[1], and Runsheng Wang[2]** [1]Nexchip Semiconductor Corporation, China; [2]Peking University, China
17:30	7773	**RBGR: Backward-Only Residual Gradient Reweighting for Robust Analog CIM Inference** **Yizhe Chen[1,3], Yuxin Xie1, Xiaofei Hu[3], Yuannuo Feng[1,3], Ngai Wong[2], Wenyong Zhou*[2,3], and Wang Kang*[1]** [1]Beihang University, China; [2]The University of Hong Kong, China; [3]Zhicun Research Lab, China

Technical Session 09: Power Devices & Power IC-II

Time	16:00-17:50, October 28, 2026	Venue	Yuqing Hall
Session Chair	Hengyu Wang, Zhejiang University, China		

Session Details		
16:00	Invited	**Novel structures for high-stable enhancement mode pGaN gate GaN Power Devices** **Qimeng Jiang** Southwest Jiaotong University, China
16:20	Invited	**Novel High Voltage Gallium Oxide Power Devices with Heterojunction Field Plates** **Jie Wei** University of Electronic Science and Technology of China, China
16:40	Invited	**Wireless Power Transfer or Isolated Converter** **Yang Liu** Xidian University, China
17:00	Invited	**High-Voltage GaN Power Devices and Modeling Techniques** **Kemeng Yang** Nanjing University of Posts and Telecommunications, China
17:20	1848	**Impact of Total Ionizing Dose Irradiation and Gate Switching Stress-Induced Degradation on Silicon Carbide MOSFETs** **Tengkun Luo[1], Xiaochuan Deng*[1], Jiahao Hu[1], Tao Xu[1], Yuewei Guo[2], Lei Duan[2], Jiaqi Zhang[2], WenYi[1], Xuan Li[1], Bo Zhang[1]** [1]University of Electronic Science and Technology of China, China; [2]Hebei Bowei Integrated Circuits Co., Ltd., China
17:35	3489	**High-Temperature Characterization of CMOS Devices and Basic Circuits on a Discrete-Device-Compatible 4H-SiC Integrated Platform** **Yawen Xu[1], Yong Gu[1], Xuye Zhang[1], Jiaqi Wang[1], Haitao Huang[2], Jie Ma*[1], Long Zhang*[1], Siyang Liu, Weifeng Sun** [1]Southeast University, China; [2] Inventchip Technology Co., Ltd., China

Technical Session 10: Digital Architectures & Systems-I

Time	16:00-18:00, October 28, 2026	Venue	Huiyuan Hall
Session Chair	Zhuojun Chen, Hunan University, China		

Session Details		
16:00	3945	**A Heterogeneous Acceleration System for Minimap2 Long-Read Sequence Mapping** **Jingcheng Hu[1], Jialei Sun[1], Xinrui Zhang[1], Xuefei Ming[2], Shuli Liu[2], Jianfei Jiang*[1]** [1]Shanghai Jiao Tong University, China; [2] The 58th Research Institute of China Electronics Technology Group Corporation, China
16:15	8545	**CryptX-IF: A Tightly-Coupled Application-Specific Instruction Processor with the RISC-V K-Extension** **Jungeng Shi[1], Bo Chen[1], Xuxiang Wang[1], Yao Liu[1,2,3,*]** [1]Sun Yat-sen University, China; [2]Fudan University, China; [3]Guangdong Provincial Key Laboratory of Advanced Integrated Circuit Design and Integration Technology, China
16:30	3566	**Repair Scheme for LUT in SRAM-Based FPGA** **Cong Xu[1,2], Fan Yang[1], Ning Song[2], Xingsheng Wang[1*]** [1]Huazhong University of Science and Technology, China; [2]Gowin Semiconductor Corporation, China
16:45	4169	**An AES Algorithm with Dynamic S-Boxes Generated by APUF Obfuscation** **Zhenkai Zhou[1], Shuang Hu[1], Yuejun Zhang[1], Dameng Dai[2], Pengjun Wang*[2]** [1]Ningbo University, China; [2]Wenzhou University, China
17:00	0117	**Content-Adaptive and Temporally Stable Compressive Sensing via Row-Nested Binary FPGA Encoding** **Jiaqi Zhong, Zhixing Zhao, Qiang He, Yudi Zhao*, Kai Zhao** Beijing Information Science and Technology University, China
17:15	8568	**NoAlloc-TLB: A TLB Protection Mechanism Against Speculative Execution Attacks** **Junhui Wang[1,2'†], Shiyuan Wang[1,2'†], Jiawei Gong[1,2], Jierong Tang[1,2], Jiahong Liu[1,2], Haoming Jia[1,2], Li Luo*[1,2]** [1]National University of Defense Technology, China; [2]Key Laboratory of Advanced Microprocessor Chips and Systems, China
17:30	6054	**A RISC-V Coprocessor for Accelerating the PERK Post-Quantum Digital Signature Scheme** **Ruoling Ma[1], Xinglong Yu[1], Yifan Zhao[1], Chao Fu[2], Jun Han*[1]** [1]Fudan University, China; [2]Fudan University, China
17:45	9177	**A gm/IDS-Based Design Methodology to Define the Optimum Bias Point of Half-Diamond and Rectangular MOSFETs for Single-Transistor Voltage Amplifiers** **Egon H. S. Galembeck*[1], Cor Claeys[2], Fellow, IEEE, Denis Flandre[3], Senior Member, IEEE, and Salvador P. Gimenez[1], Senior Member, IEEE** [1] FEI University Center, Brazil; [2] KU Leuven, Belgium; [3] ICTEAM, Université catholique de Louvain, Belgium

Technical Session 11: CMOS Logic Devices & Sensors-I

Time	16:00-18:00, October 28, 2026	Venue	Yaxu Hall
Session Chair	Heng Wu, Peking University, China		

Session Details		
16:00	Keynote	**2D Bismuth Oxyselenide for Future Electronics** **Hailin Peng** Peking University, China
16:30	Invited	**Reliability Design in QLC High Bit-Density 3D NAND Flash** **Jiezhi Chen** Shandong University, China
16:50	Invited	**Technology Development of Low Temperature CMOS: Process, PDK, and Reliability** **Ran Cheng** Zhejiang University, China
17:10	Invited	**Thermally-Aware Reliability Engineering for Advanced Logic and Heterogeneously Integrated Systems** **SangHoon Shin** Hanyang University, South Korea
17:30	8297	**High-Contrast Impedance-Based Droplet Position Sensing for Active-Matrix Digital Microfluidics** **Yong Le[1], Yan Huang[1], Congwei Liao[2], Shengyou Zhang[1], Shengdong Zhang*[1,3]** [1]Peking University, China; [2] Shenzhen Technology University, China; [3]Shenzhen Polytechnic University, China
17:45	6136	**Silk-Fibroin Composite Micro-Sensor for Active Multimodal Wearable Sensing** **Hao Zheng[1], Yaoyao Li[1], Yu Chen*[1], Xiaosheng Zhang*[1]** [1] University of Electronic Science and Technology of China, China

Technical Session 12: Optoelectronics and Silicon Photonics Integration-I

Time	16:00-17:50, October 28, 2026	Venue	Shuibo Hall
Session Chair	Linfeng Sun, Beijing Institute of Technology, China		

Session Details		
16:00	Invited	**Phase Change Materials-integrated Nonvolatile Reconfigurable Photonics** **Junying Li** University of Chinese Academy of Sciences, China
16:20	Invited	**The Computational Silicon Photonic Spectrometers** **Tong Lin** Southeast University, China
16:40	Invited	**2D Van Der Waals Metal Phosphorus Trichalcogenides for Photodetector and Memristor Applications** **Zhengjin Weng** Jiangnan University, China
17:00	Invited	**High-Performance Short-Channel p-Type Monolayer WSe2 Transistors** **Xuefei Li** Huazhong University of Science and Technology, China
17:20	5667	**Electric-Field Redistribution and Self-Limited Tunneling in MoTe2/hBN/Graphene Floating-Gate Memory** **Ce Li[1], Mingyue Yuan[1], Zirui Zhang[1], Linfeng Sun[1]*** [1]Beijing Institute of Technology, China
17:35	8035	**Electrode-Geometry-Dependent Spatial Photocurrent and Transient Response in Layered MoWS4 Alloy Photodetectors** **Qixin Deng[1], Xun Zhao[2], Jiaxu Yan*[2], Linfeng Sun*[1]** [1]Beijing Institute of Technology, China; [2]Chinese Academy of Sciences, China

Technical Session 13: Packaging Technologies

Time	16:00-18:00, October 28, 2026	Venue	Tianhan Hall
Session Chair	Jun Zhang, Nanjing University of Posts and Telecommunications, China		

Session Details		
16:00	Invited	**Application & Challenges of Advanced Packaging in NPO/CPO** **Hong Xie** HuaMao Technology, China
16:20	Invited	**The Requirements of Silicon Substrate for Advanced Packaging Applications** **Tian Feng** National Silicon Industry Group, China
16:40	Invited	**A Brief Discussion on Standardization Issues in the Assembly and Testing Industry** **Junjie Wang** Changjing Technology, China
17:00	5013	**Effect of Phosphorus Content in Ni-P Coatings on the Soldering Performance of AMB Substrates for Power Device Packaging** **Jinlong Yang*[1, 2], Jian Luo[1, 2], Feng Xiong[1, 2],** [1]Nanjing NARI Semiconductor Co., Ltd., Nanjing, China; [2] State Grid Electric Power Research Institute (NARI Group Co., Ltd.), Nanjing, China
17:15	5231	**Thermal-Aware Design-Space Exploration of Microfluidic-Cooled 3D ICs** **Mingyue Dong, Wangyong Chen*, Haoyu Zhang, Linlin Cai** Sun Yat-sen University, China; Zhuhai Key Laboratory of Intelligent EDA and Reliability Design of Advanced Integrated Circuits, China
17:30	1014	**Dynamic Finite Element Analysis of the Back Grinding Stress for TSV Wafers Supported by Cap Wafer with Silicon Cavities** **Beilin Ouyang*[1], Xiaodan Li[1], Xiangyang Shi[1], Yaning Lin[1], Rong Zeng[1], YuanPeng Li[1]** [1]China of Academy Engineering Physics, China
17:45	9351	**Hierarchical Reduced-Order Modeling of TSV Thermal–Mechanical Systems via POD–SINDy** **Ziyong Wang, Weizhi Li, Yaojie Mo, Haoyu Zhang, Yunlong Zhang, Linlin Cai, Wangyong Chen*** Sun Yat-sen University, China; Zhuhai Key Laboratory of Intelligent EDA and Reliability Design of Advanced Integrated Circuits, China

Technical Session 14: General Analog-II

Time	13:30-15:25, October 29, 2026	Venue	Huanying Hall
Session Chair	Junmin Jiang, Southern University of Science and Technology, China		

Session Details		
13:30	Invited	**A Capacitively-Biased Diode Technique and Its Applications** **Zhong Tang** Hangzhou Institute of Technology, Xidian University, China
13:50	Invited	**Towards Flexible Biomedical Systems: Circuits and Design on Thin-film Transistors** **Jian Zhao** Shanghai Jiao Tong University, China
14:10	5616	**A 120×120 CMOS Image Sensor with Programmable Block-level Regions-of-interest for Data Reduction** **Xinpeng Li[1, 2], Yandong He[1, 2], Gang Du*[1, 2]** [1]Peking University, China; [2]Beijing Advanced Innovation Center of Integrated Circuits, China
14:25	6005	**A Single-Controller Adaptive-Conduction-Mode Photovoltaic Energy Harvester for Simultaneous MPPT and Output Regulation** **Yukai Zhang[1], Jiafeng Liu[1], Tao Wang [1], Xufeng Liao[1,2] and Lianxi Liu*[1,2]** [1]Xidian University, China; [2] Xidian University Chongqing ICs Innovation Institute, China
14:40	9724	**A Slew-Rate-Boosted Time-Multiplexed C/V Converter for MEMS Capacitive Sensors with Large Parasitics** **Jun Feng[1,2], Yuchen Wang[1,2], Yongmeng Zhang*[1,2], Dingbang Xiao*[1,2]** [1]National University of Defense Technology, China; [2] National University of Defense Technology, China
14:55	9822	**A 40-nm CMOS Laser Diode Driver With Chopper-Stabilized Bias Regulation for FMCW LiDAR** **Shangqi Wu [1], Tenglong Ke[1], Keping Wang*[1]** [1]Tianjin University, China
15:10	7717	**A 300 MS/s, 14-Bit Pipelined-SAR ADC Using PVT-Robust Ring Amplifier with CMFB Circuit** **Tianyu Zhai [1], Linghao Liu [1], Fan Ye*[1]** [1]Fudan University, China

Technical Session 15: Power Devices & Power IC-III

Time	13:30-15:05, October 29, 2026	Venue	Yuqing Hall
Session Chair	Pengyu Lai, Southeast University, China		

Session Details		
13:30	Invited	**High-voltage E-mode GaN Transistors for Efficient Power Switching Applications** **Huaxing Jiang** South China University of Technology, China
13:50	Invited	**Interface-Dependent Gate Reliability and Trap Dynamics in GaN FinFETs** **Wen Yang** South China University of Technology, China
14:10	Invited & 3527	**Novel Air-Gap Self-Shielding 1200 V HVIC with an Enhanced Isolation Breakdown Voltage** **Guoliang Yao** Hangzhou Silan Microelectronics Co., Ltd., China
14:30	Invited & 6519	**Large Language Model-Based Yield Enhancement and Prediction Methodology in Wafer Fabrication** **Yawei Chen** China Resources Microelectronics Ltd., China
14:50	9728	**Monolithic GaN Comparator with an Extended Input Range and Balanced Propagation Delays Enabled by Asymmetric-Load Topology** **Wenxin Zhu[1], Yudong Li[1], Haowei Zhang[1], Xuanling Zhou[1], Jietong Li[1], Xinbo Zou*[1]** [1]ShanghaiTech University, China

Technical Session 16: CMOS Logic Devices & Sensors-II

Time	13:30-15:30, October 29, 2026	Venue	Huiyuan Hall
Session Chair	Xiaosheng Zhang, University of Electronic Science and Technology of China, China		

Session Details		
13:30	Keynote	**Integrated Chip Based Frequency-Locking Technology for Ultrasonic Systems: Multi-Physics Effects and Engineering Applications** **Linxi Dong** Hangzhou Dianzi University, China
14:00	Invited	**Research on Key Technologies of CMOS Three-Axis Hall Sensors** **Hua Fan** University of Electronic Science and Technology of China, China
14:20	Invited	**Integration Challenges for On-chip Backside Power Delivery** **Han Li** Southeast University, China
14:40	Invited	**Overcoming the Physical Limits of Silicon Transistor Downscaling** **Junwei Luo** Chinese Academy of Sciences, China
15:00	4599	**Self-Selective Pt/Ta2O5/TiN Memristor for Biomimetic Artificial Nociceptor** **Jie Wang[1], Zijian Wang[1], Guobin Zhang[1], Qi Luo[1], Haoze Yu[1], Yishu Zhang*[1]** [1]Zhejiang University, China
15:15	1799	**Study of Global Stress Impact on 14 nm FinFET Toward Hybrid-bonding 3D Logic** **Xuanyu Jia[1], Xijun Zhou[1], Haoran Zhao[1], Xiaoyan Xu[1,2], Xia An[1,2] and Ming Li[1,2*]** [1]Peking University, China; [2]Beijing Advanced Innovation Center for Integrated Circuits, China

Technical Session 17: Device Reliability & Security-II

Time	13:30-15:15, October 29, 2026	Venue	Yaxu Hall
Session Chair	Xuanze Zhou, University of Science and Technology of China, China		

Session Details		
13:30	Invited	**Defect Characterization and Carrier Transport Control in GaN Devices** **Yixu Yao** Chinese Academy of Sciences, China
13:50	Invited & 7577	**From Remote Heat Sinks to Hotspot-Proximal Cooling: A Review of Near-Junction Thermal Management Strategies for GaN Power Devices** **Wei Jia ZHANG** The Hong Kong University of Science and Technology, China
14:10	Invited	**Atomistic Understanding and Control of Dislocations in Nitride Semiconductors** **Han Yang** Peking University, China
14:30	9973	**Investigation of Single-Event Burnout Robustness in GaN HEMTs with AlGaN Back-Barriers** **Kaiwei Zhang[1,2], Chenrui Zhang[1,2], Jianfei Liu[1,2], Yixu Yao[1,2,*], Li Yu[1,2], Xinhua Wang[1,2], MingyanWang[1,2], Yi Pei[3], Hongtu Qian[3], Baikai Zhang[3], Hui Zhang[3], Xinyu Liu[1,2], Yuxuan Xiang[4], Jun Zhang[4], and Sen Huang[1,2,*]** [1]Chinese Academy of Sciences, China; [2]University of Chinese Academy of Sciences, China; [3] Dynax Semiconductor, China; [4]Nanjing University of Posts and Telecommunications, China
14:45	8052	**Physics-Informed LSTM with Static Parameter Inversion for Long-Term Prediction of Dynamic Ron in GaN HEMTs** **Jingyun Guan, and Wen Yang[*]** [1]South China University of Technology, China
15:00	2205	**Experimental Characterization of Improved Single-Event Radiation Tolerance in 700 V Split-SJ LDMOS** **Jian Chen[1], Teng Liu[1], Anna Zhang[2], Shenghuai Liu[1*], Jian Xu[1], Yujing Fu[1], Hao Wang[2], Xin Zhang[2], Zeyu Bian[3], Zilong Wang[3], Shuai Cui[3], Xin Zhou[1], Wentong Zhang[1*] and Bo Zhang[1]** [1]University of Electronic Science and Technology of China, China; [2] Wuxi CR Huajing Microelectronics Co., Ltd., China; [3]Chinese Academy of Science, China

Technical Session 18: RF & Wireless-II

Time	13:30-15:25, October 29, 2026	Venue	Shuibo Hall
Session Chair	Jian Pang, Shanghai Jiao Tong University, China		

Session Details		
13:30	Invited	**High-Efficiency Sub-7 GHz Digital Power Amplifier and Transmitter With Intrinsic Harmonic Suppression** **Bingzheng Yang** Shenzhen University, China
13:50	Invited	**Where RFIC Meets AI: From Semantic to Silicon** **Francois Rivet** University of Bordeaux, France
14:10	Keynote	**Terahertz Phased-Array Transceiver Design in 65nm CMOS** **Chun Wang** Zhejiang University, China
14:40	7588	**An 8-to-16 GHz Low-Coupling Ultra-Wideband VCO with 8-Shaped Transformer-Loaded Inductor in 65-nm CMOS** **Chaoping Feng†, Sihan Li†, Hongzhi Wu, Quan Pan*** Southern University of Science and Technology, China
14:55	5462	**A 60 GHz CMOS Transmitter Utilizing 6-Bit Active Phase Shifter for Phased Array Application** **Fei He[1, 2*], Ji Dong[1], Xincong Wang[1], Shoulin Wang[1], Pengkun Fan[1], Haonan Dang[1]** [1] Chongqing Giga Chip Technology Co. Ltd.; [2] CETC No. 24 Research Institute
15:10	6698	**A 9.16-to-10.72 GHz Compact Inductor-based Series Resonance VCO with Folded 8-shaped Inductor Achieving 195.4dBc/Hz FoMA at 10 MHz Offset** **Ruidong Ye, Jinhua Guo, Pei Qin*** South China University of Technology, China

Technical Session 19: Digital Architectures & Systems-II

Time	13:30-15:35, October 29, 2026	Venue	Tianhan Hall
Session Chair	Amara Amara, International Innovation Institute, Beihang University, Hangzhou Campus, China		

Session Details		
13:30	Keynote	**From Reliable Bits to Reliable Intelligence: Energy-Efficient and Reliable Networks-on-Chip for AI** **Fakhrul Zaman Rokhani** Universiti Putra Malaysia, Malaysia
14:00	Invited	**Chiplet Based Near/In Memory Computing** **Letian Huang** University of Electronic Science and Technology of China, China
14:20	0152	**DTCO-Driven Standard and Complementary SOT-MRAM Macros for High Density and Superior Write Performance** **Xiaoyang Xu[1,2], Shaohui Ma[1,2], Shangyu Li[1,2], Zhongzhen Tong[1], Chenhan Cui[2], Chenyi Wang[1,2], Lang Zeng[2], Chao Wang[1,*], and Zhaohao Wang[1,2,4,3]** [1]Hangzhou International Innovation Institute, Beihang University, Hangzhou, China; [2]Beihang University, China; [3]Shandong Laboratory of ASIC and Intelligent Instruments in Qingdao, Beihang University, Qingdao, China
14:35	7965	**A Novel Three-Dimensional Heterogeneous SoC Design Based on Logic Folding** **Shuoqi Fu[1], Yuan Zhuang[1], Xuefei Ming[2], Shuli Liu[2], Qin Wang[1], Jianfei Jiang*[1]** [1]Shanghai Jiao Tong University, China; [2] The 58th Research Institute of China Electronics Technology Group Corporation, China
14:50	8604	**A Profiling-Guided Reconfigurable RISC-V Coupled Coprocessor for Multi-Standard PQC** **Wenbo Xu[1], Yong Zhang[2], Fan Zhang[2], Jiayi Li[*1], Jinyan Luo[*1], Jiahao Lu[1], Zhengpeng Zhao[1], Dongsheng Liu[*1]** [1]Huazhong University of Science and Technology, China; [2]Hubei Siant Science & Technology Co., Ltd., China
15:05	7929	**An HLS-Based Pipelined FPGA Accelerator for Temporal Fusion Transformer** **Yiwei Wang[1], Zehao Wu[2], and Chang Wu[1,*]** [1]Fudan University, China; [2]HillSide Technologies Co. Ltd., China
15:20	9055	**Resource Transformation for Fast FPGA Inference** **Bakhtiar Zadeh[*], Kevin Halm Alvarez[*], Chang Sun[†], Wayne Luk[*], Zhiqiang Que[*‡]** [*]Imperial College London, UK; [†] California Institute of Technology, USA; [‡] University of Bristol, UK

Technical Session 20: Optoelectronics and Silicon Photonics Integration-II

Time	16:00-17:45, October 29, 2026	Venue	Qinglian Hall
Session Chair	Yuanfang Yu, Jiangnan University, China		

Session Details		
16:00	Invited	**Multi-dimensional Light Field Detection based on Carrier Dynamics Modulation in Two-dimensional Devices** **Yuanfang Yu** Jiangnan University, China
16:20	Invited	**Exploring Thermoelectric Pathways in 2D Integrated Photodetectors** **Peng Xiao** Jiangnan University, China
16:40	Invited	**Infrared Light-emitting Devices Based on 2D Semiconductors for Silicon Photonics** **Junyong Wang** Suzhou Institute of Nano-Tech and Nano-Bionics (SINANO), CAS, China
17:00	6800	**Design of a Linear Absolute Optical Encoder Readout Chip With a Reconfigurable Regional Reference Network** **Zhiqi Geng [1], Dongning Hao [1]*, Jiarong Li [1], Wei Zhang [1]** [1]Tianjin University, China
17:15	7110	**Photomemory-Enabled ZTO TFT as a Single-Device Temporal Optical Encoder for Spike-Based Neuromorphic Readout** **Yiwen Wang[1,†], Junxu Tao[1,†], Yanming Kuang[1,†], Yitian Li1, Ruohan Li[1], and Chun Zhao[1,*]** [1]Xi'an Jiaotong-Liverpool University, China; [†]These authors contributed equally to this work
17:30	2442	**LIGHTCOMMIT: Hardware-Enforced Cross-Domain Transaction Suppression in Photonic SNN Accelerators** **Junxu Tao[1], Jiayan Zhang[1], Mochi Pan[2], Zhengtao Yuan[1], Chun Zhao[1,*] and Jiaqi Liu[1,*]** [1]Xi'an Jiaotong-Liverpool University, China; [2]University of Liverpool, UK

Technical Session 21: Design Methodology & EDA-II

Time	16:00-18:15, October 29, 2026	Venue	Huanying Hall
Session Chair	Pengying Chang, Beijing University of Technology, China		

Session Details		
16:00	Keynote	**Simulation and Design Space Exploration for Integrated Chip-Systems** **Xiaohang Wang** Zhejiang University, China
16:30	9212	**An Automated Hardware-Aware Precision-Recovery Framework for Deep Learning Deployment on Compute-in-Memory Accelerators** **Chenyu Liang[1], Yizhe Chen[2]** [1]Shenzhen International Graduate School, Tsinghua University, China; [2]Beihang University, China
16:45	4987	**PINN-Based Inverse-Design Agent for Semiconductor Devices with Ultra-Small Datasets** **Liang Li[1,2,3], Zeheng Wang[1,2,*], Zhuocheng Wang[4], Cheng Yu[5], and Fangzhou Wang[4,*], Genquan Han[1,2]** [1]Hangzhou Institute of Technology, Xidian University, Hangzhou, China; [2]Xidian University, China; [3] Peking University, China; [4]Shenzhen Institute for Advanced Study, UESTC, Shenzhen, China; [5]Songshan Lake Materials Laboratory, China
17:00	5473	**PIF: Black-Box Process-Level Parallel Logic Optimization for FPGA Synthesis** **Yuping Bai, Kaixiang Zhu, and Lingli Wang*** Fudan University, China
17:15	9710	**A Selected-Fanout Bypass Method for Post-CTS Backside Clock ECO** **Xiaolian Lin[1], Yang Shen[1], Bingyi Ye[1], Xiaojin Li[1], Yabin Sun[1], Yuhang Zhang*[1]** [1]East China Normal University, China
17:30	5636	**A Level-Wise Parallel Framework for LUT Mapping in ABC** **Zixuan Xiao[1], Zhengyi Zhang[1], and Lingli Wang[1,*]** [1]Fudan University, China
17:45	0578	**Input-Vector-Dependent Aging-Aware Path Timing Prediction for Reliable Advanced CMOS Circuits Using Hybrid Graph Learning** **Runsheng Liu, Zhibin Chen, Songxuan He, Linlin Cai*, Wangyong Chen*** Sun Yat-sen University, Guangzhou, China; Zhuhai Key Laboratory of Intelligent EDA and Reliability Design of Advanced Integrated Circuits, China
18:00	4366	**New Framework on Model-Based System Reliability/Yield-Aware Design towards τ-Scaling** **Zhuoqing Yu*, Yongsheng Sun, Chenghuan Wen, Jianchao Hu, Xiaowei Lin, Zhen Chen** Huawei Technologies Co., Ltd., China

Technical Session 22: Power Devices & Power IC-IV

Time	16:00-17:45, October 29, 2026	Venue	Yuqing Hall
Session Chair	Pengyu Lai, Southeast University, China		

Session Details		
16:00	Invited	**Buck Converter Verification Based on Optimized Monolithic Heterogeneous GaN/Si CMOS Integration** **Wei Huang** Jiangnan University, China
16:20	Invited	**SiC CMOS IC for Future Power Electronics and Harsh Environment Applications** **Zhong Chen** The Hong Kong Polytechnic University, China
16:40	Invited	**A Novel Bevel-Terminated SiC Floating-Junction Device with Improved Turn-on Recovery Characteristics** **Hao Yuan** Xidian University, China
17:00	9133	**Comparative Analysis of Hot-Carrier Degradation Physics in SOI-LDMOS Featuring Trench Isolation** **Dejin Wang[1,2], Teng Liu[2], Nailong He[1,2], Jingchuan Zhao[2], Zhili Zhang[2], Lin Bai[2], Sen Zhang[2], Jie Ma[1], Long Zhang[1], Shiyang Liu[1] and Weifeng Sun[1*]** [1]Southeast University, China; [2]Technology Development Department, CSMC Technologies Corporation, China
17:15	1303	**A Quasi-Constant Frequency DC-DC Converter Controller Based on Ultra-fast Duty Sampling Technique for Rapid Frequency Regulation** **Yujie Fan[1], Xinyang Liu[1], Shidong Wang[1], Yue Shi[2*], Zekun Zhou[1], Bo Zhang[1]** [1]University of Electronic Science and Technology of China, China; [2]Chengdu University of Information Technology, China
17:30	6601	**A Novel 2000 V Lateral Power Device With Multi-Dimensional Junction Modulation** **Nailong He[1,2*], Shixiong Chong[2], Teng Liu[2], Jian Chen[2], Xiaofeng Lai[2], Yongshun Li[2,4], Lihui Gu[2], Yuheng Yao[2], Yongyu Shi[2], Changfeng Xia[3], Dejing Wang[2], Sen Zhang[2], Jie Ma[1], Long Zhang[1],Shiyang Liu[1] and Weifeng Sun[1*]** [1]Southeast University, China; [2]Technology Development Department, CSMC Technologies Corporation, China; [3]Jiangsu Provincial Key Laboratory of MEMS Sensors and ASIC Manufacturing Technology, China

Technical Session 23: CMOS Logic Devices & Sensors-III

Time	16:00-17:25, October 29, 2026	Venue	Huiyuan Hall
Session Chair	Wangyong Chen, Sun Yat-sen University, China		

Session Details		
16:00	Invited	**Key Technology Investigations of GAA and CFET Devices** **Jun Luo** Chinese Academy of Sciences, China
16:20	Invited	**From "Vision Sensing Is Computing" to "Light Propagation Is Computing": Exploring Optoelectronic AI Architectures** **Liang Ran** Pixelcore, China
16:40	2656	**Low-Frequency Noise Characteristics of EMMO TFTs Under Illumination Stress** **Baoqiong Fu[1], Yuwei Zhao[1], Bo Wang[1], Lei Lu[2], Man Wong[3], Hoi-Sing Kwok[3], Meng Zhang*[1]** [1]Shenzhen University, China; [2]Shenzhen Graduate School, Peking University, Shenzhen, China; [3]The Hong Kong University of Science and Technology, China
16:55	9607	**Compact Modeling of Gate-Fringe Parasitic Capacitance for Three-Stack Nanosheet Reconfigurable FETs** **Mengge Jin[1], Fu Gong[1], Xiaojin Li[1], Yang Shen[1], Bingyi Ye[1], Ziyu Liu[2], Yuhang Zhang[1] and Yabin Sun*[1]** [1] East China Normal University, China; [2] Fudan University, China
17:10	8150	**Ti-Capped Electrode and CMP Treatment Interface Planarization for Endurance-Enhanced Sub-10 nm HfZrO Ferroelectric Capacitors** **Xiaolin Jiang[1], Zihao Guo[1], Qian Cheng Yang[1], Shenglin Pan[1], Jialong Xiang[1], Zhibo Zeng[1], Dun-BaoRuan[1*]** [1] Fuzhou University, China

Technical Session 24: Device Reliability & Security-III

Time	16:00-18:00, October 29, 2026	Venue	Yaxu Hall
Session Chair	Sen Huang, Chinese Academy of Sciences, China Jiangbin Wu, Chinese Academy of Sciences, China		

Session Details

16:00	Invited	**Development of Extremely Low on-Resistance AlN-based Schottky Barrier Diodes** **Takuya Maeda** The University of Tokyo, Japan
16:20	Invited	**Vertical Nitride Power Devices: from wide-bandgap to ultra-wide-bandgap semiconductors** **Chao Liu** Shandong University, China
16:40	Invited	**Thermally Stable p-GaN/n-Ga2O3 Heterojunction Termination for High-Voltage Fully Vertical β-Ga2O3 Schottky Barrier Diodes** **Bin Hou** Xidian University, China
17:00	7005	**Total-Ionizing-Dose Radiation Effect on VTH Instability of Schottky-Type p-GaN Gate HEMTs Under Dynamic Gate Bias** **Shuting Huang[1], Jianggen Zhu[1], Qinqin Yang[1], Fukang Yang[2], Jinggui Zhou[1], Xin Zhou[1], Bo Zhang[1]and Qi Zhou*[1,2,3]** [1] University of Electronic Science and Technology of China, China; [2] Shenzhen Institute for advanced study, UESTC, Shenzhen, China; [3] Institute of Electronic and Information Engineering in Dongguan, UESTC, Dongguan, China
17:15	5000	**Multiple Scale Physical Analysis of HAST-Induced Degradation in Advanced MIM/STK Capacitors** **Yu Yao[1], Jingming Zhou*[1,2], Chen Chang[3], Jialu Huang[1], Xing Wu[1]** [1]East China Normal University, China; [2]Peking University, China; [3]Maxscend Microelectronics Company Limited, China
17:30	6551	**Silicon Controlled Rectifier for ESD Protection of TFET-MOSFET Hybrid Technology** **Zhaonian Yang*[1], Tongbo Gao[1], Leiming Zhu[1], Yuwen Zhang[1], Yuan Yang[1], Zhigang Ji[2]** [1]Xi'an University of Technology, China; [2]Shanghai Jiao Tong University, China
17:45	4073	**A Threshold-Loss Based Arbiter PUF with Delay-Deviation Encoding** **Tianyi Xiao[1], Xilong Shao[1], Gang Li*[2], and Xuejiao Ma[3]** [1]Wenzhou University, China; [2]Fudan University, China; [3]Wenzhou University of Technology, China

Technical Session 25: Semiconductor Process Technologies-II

Time	16:00-17:45, October 29, 2026	Venue	Shuibo Hall
Session Chair	Han Li, Southeast University, China		

Session Details		
16:00	3857	**Polarization Enhanced E-mode GaN p-channel MOSFET on the P-GaN/UID-GaN/AlN Platform** **Yifan Gao [1], Ling Yang*[1], Bin Hou [1], Mei Wu [1], Meng Zhang [1], Hao Lu [1], Xiaohua Ma [1]** [1]Xidian University, China
16:15	5618	**Research on the Application of Decoupled Plasma in Surface Treatment of PEALD-Grown Silicon Dioxide Layers** **Jichu Zhang [1], Dedong Han*[1]** [1] Peking University, China
16:30	8867	**Analysis of LER Impact on Nanosheet GAAFETs** **Yajuan Su[1,2,3,*], Xin Hong[1,2,3], Xiaojing Su[1,2,3], Yuqin Wang[1,2,3], Pengyu Ren[1,2,3], Yujie Jiang[1,2,3], Fanqian Meng[1,2,3], Jiarong Yang[1,2,3], and Yayi Wei[1,2,3,*]** [1]University of Chinese Academy of Sciences, China; [2]Chinese Academy of Sciences, China; [3]State Key Laboratory of Fabrication Technologies for Integrated Circuits, China
16:45	9562	**TCAD-Based Co-Optimization of S2G and Seed Layer Coverage for eSiGe PMOS Devices** **Xiuqi Li[1], Shiyou Chen*[1]** [1]Fudan University, China
17:00	3957	**Experiment-Calibrated Multi-Stage Current Waveform Optimization for Copper Electroplating and CMP on Glass Substrates** **Chuping Zhang[1], Miao Tian[1], Peiyi Yang[1], Yan Zhong[1], Xiaojun Guo*[1], Zhuoqing Yang*[1]** [1] Shanghai Jiao Tong University, China
17:15	7369	**Engineer-Experience-Driven Discovery and Physical Verification of S/D Recess-Induced Ioff Outliers in 28 nm Core Devices** **Yangyang Bao[1]*, RR Zhu[1], Yuri Ma[1], Levi Chen[1], Junun Zhu[1], Chih-Wei Lin[1], Chih-Peng Liang[1], Yi-Chuen Eng[1]*, Daiki Qin[1], Po-Ju Chen[1], Zhe-Ju Liu[1], Wendy Wang[1], Bo Liu[1], Chih-Ying Chan[1], Jhong-Sheng Wang[1], and Chia-Yen Li[1]** [1]Nexchip Semiconductor Corporation, China
17:30	9671	**Depletion-to-Enhancement Mode Transition in InSnO/ZnO Thin-Film Transistors via InSnO Gate Work-Function Modulation** **Kuan Yin[1], Junchen Dong*[1], Chuanlin Sun[2], Dedong Han[2]** [1]Beijing Information Science & Technology University, China; [2]Peking University, China

Technical Session 26: Digital Circuits-II

Time	16:00-17:45, October 29, 2026	Venue	Tianhan Hall
Session Chair	Eimer Sylvain, Beihang University, China		

Session Details		
16:00	4409	**A 40.41 TOPS/W Time-Domain Computing-in-Memory Macro With Delay Calibration and Zig-Zag Power Gating** **Xiongyu Chen[1,2], Ke Wu[1,2], Yuekang Guo[1,2], Jing Jin[1,2*]** [1]Shanghai Jiao Tong University, China; [2]SJTU-Montage IC Design Frontier Technology Joint Laboratory, China
16:15	9733	**A Clock-Data Synchronization Circuit for x64 D2D Links in 28-nm CMOS** **Shuaipeng Li[1], Lin Xie[1], Sai Gao[1], Xuefei Ming[2], Shuli Liu[2], Jianfei Jiang*[1]** [1]Shanghai Jiao Tong University, China; [2] The 58th Research Institute of China Electronics Technology Group Corporation, China
16:30	3551	**A CPU-GPU-FPGA Architecture for Low-Batch Multimodal Video Inference** **Ziyao Wang[1], Kunyue Li[1], Xuefei Ming[2], Shuli Liu[2], Jianfei Jiang*[1]** [1]Shanghai Jiao Tong University, China; [2] The 58th Research Institute of China Electronics Technology Group Corporation, China
16:45	1458	**A Voltage-Stacked Power Delivery System for 3D Many-Core Architectures** **Jiayu Zhou[1], Xuefei Ming[2], Shuli Liu[2], Jianfei Jiang*[1]** [1]Shanghai Jiao Tong University, China; [2] The 58th Research Institute of China Electronics Technology Group Corporation, China
17:00	2907	**COAST: Hardware-Algorithm Co-Design with Dynamic Workload Allocation for 3D-DRAM and SRAM-CIM Stacked LLM Accelerator** **Haoyu Zhang[†], Yifan Wu[†], Liukai Xu, Yunhao Xiong, Yanan Sun[*]** Shanghai Jiao Tong University, China
17:15	2992	**A New High-Accuracy and Area-Efficient 2-Term Floating-Point Fused Dot-Product Unit** **Yufei Wan, Zelong Yuan, Lei Xu, Dongyan Liu, Chen Yin[*], Naifeng Jing** Shanghai Jiao Tong University, China
17:30	0009	**An Ultra-Low-Latency BP-OSD Decoder for Quantum Error Correction Codes** **Changfu He[1], Jielun Xu[2], Suwen Song[*2], Lang Feng[2], and Zhongfeng Wang[*1,2]** [1]Nanjing University, China; [2]Sun Yat-sen University, China

Technical Session 27: General Analog-III

Time	09:00-10:15, October 30, 2026	Venue	Qinglian Hall
Session Chair	Weihong Xu, Zhejiang University, China		

Session Details		
09:00	9790	**Design of a Low-Power High-Speed PWM Comparator and a High-CMTI Level Shifter for a High-Voltage Buck Power Management Circuit of BMS in EV** **Zhuo Li [1], Liji Wu*[2], Zhiyuan Li*[1], Xiangmin Zhang[2]** [1]Heilongjiang University, China; [2]Tsinghua University, China
09:15	4671	**Dual Capless LDOs for an Optically Powered Sensing and μLED Communication IC** **Borong Zhang, Student Member, IEEE, Xing Wu, Liangjian Lyu*** East China Normal University, China
09:30	4768	**A 12-bit 4 MS/s Pseudo-Differential SAR ADC with a VCM-Free Common-Mode Compensated CDAC** **Jiahao Gao[1,2], Yulin Zhang*[1,2], Ye Zhao*[1,2], Shushan Qiao*[1,2]** [1]Chinese Academy of Sciences, China; [2] University of Chinese Academy of Sciences, China
09:45	7205	**A 12-bit 2.6-MSps Flash-SAR Hybrid ADC with Misplacement-Tolerant Encoding Technique** **Run-Guo Lin[1,3], Run-Kun Zhu[2], Wei-Xin Gai *[1,3]** [1]Peking University, China; [2]Beijing AKIC Technology Company Ltd., China; [3]Beijing Advanced Innovation Center for Integrated Circuits, China
10:00	1129	**An 8-GS/s 7-bit 4-Channel Time-Interleaved ADC with Power-Efficient Time-Domain Quantization and Channel Mismatch Calibration in 28-nm CMOS** **Chaoyang Zhang, Rui Gao, Yifei Gao, Yihang Yang, Runqiao Wang, Chengsen Feng, Maliang Liu*** Xidian University, Xi'an, China

Technical Session 28: CMOS Logic Devices & Sensors-IV

Time	09:00-10:15, October 30, 2026	Venue	Huanying Hall
Session Chair	Chunsheng Jiang, Guangxi Normal University, China		

Session Details

09:00	0766	**A Novel TEMAZ Treatment Technique Enabling Fine VFB Modulation and EOT Reduction for Si0.7Ge0.3 MOSCAPs** **KaiminFeng[1,2], Huaizhi Luo[1], Yongliang Li[1,2*]** [1]Chinese Academy of Sciences, China; [2]University of Chinese Academy of Sciences, China
09:15	1015	**Self-heating Effects of Flip FET Based Standard Cell and Thermal Network Model for Fast Simulation** **Naiqi Liu, Taoyu Zhou, Yandong He, Gang Du*** Peking University, China; Beijing Advanced Innovation Center for Integrated Circuits, China
09:30	8077	**Performance Optimization of Si/SiGe Monolithic CFETs Enabled by Asymmetric Inner-Spacer Engineering** **Shiqi Cao[1,2], Haoyan Liu[1], Longyu Sun[1], Yongliang Li*[1]** [1]Chinese Academy of Sciences, China; [2] University of Chinese Academy of Sciences, China
09:45	6038	**VFB Modulation and Interface Quality Improvement by La_2O_3 in a Reduced Thermal Budget Dipole-Middle Scheme** **Xingrong Xiao[1,2], Haoyan Liu[1], Yongliang Li*[1]** [1]Chinese Academy of Sciences, China; [2]University of Chinese Academy of Sciences, China
10:00	0950	**Compact Modeling of SC-RFET for Capacitorless 1T-DRAM** **Xinyu Zou[1], Bingyi Ye[1], Yuhang Zhang[1], Yang Shen[1], Xiaojin Li[1], Yabin Sun*[1]** [1] East China Normal University, China

Technical Session 29: Power Devices & Power IC-V

Time	09:00-10:15, October 30, 2026	Venue	Yuqing Hall
Session Chair	Junji Cheng, University of Electronic Science and Technology of China, China		

Session Details		
09:00	6761	**An Output-side PMOS Driver for Dual Output Boost Converter** **Han Zhou, Ping Luo*, Hao Wang** University of Electronic Science and Technology of China, China
09:15	0356	**Novel SOI-PLDMOS with Graded Drift Region and Full-Coverage Field Plate to Regulate Back-Gate Effect for Moderate-Thickness SOI Platform** **Nailong He[1*], Teng Liu[1,2], Liqi An[1], Yujing Fu[2], Ying Xiang[2], Zhuoxian Cai[2], Yongshun Li[1,2], Huajun Jin[1], Liang Song[1], Sen Zhang[1], Wentong Zhang[2*] and Bo Zhang[2]** [1]CSMC Technologies Corporation, China; [2]University of Electronic Science and Technology of China, China
09:30	6477	**A Fast and Accurate Gaussian-Function-Based Analytical Model of Multi-Epitaxial Superjunction with Experimental Verification** **Yueyu Zhang[1], Xiaofeng Lai[1], Haozhe Zhu[1], Zhuoxian Cai[1], Rongshuo Liu[1], Teng Liu[1], Longhui Lin[1], Yiduo Xie[1], Zhenyan Liu[1], Rongyao Ma[2], Ping Li[2], Tao Zhong[2], Wentong Zhang*[1], and Bo Zhang[1]** [1]University of Electronic Science and Technology of China, China; [2]China Resources Microelectronics, China
09:45	0132	**Analytical Breakdown Model for the AlGaN/GaN HEMT with the Drift Width Modulation Technique via Three-Dimensional Equivalent Method** **Zhibo Fan[1], Lingyun Zhang[1], Kemeng Yang*[1], Haowen Su[1], Liyan Gao[1], Jun Zhang*[1], HangChen[1], Jing Chen[1], Man Li[1], Jiafei Yao[1], Yufeng Guo*[1]** [1]Nanjing University of Posts and Telecommunications, China
10:00	3359	**A Non-Segmented Behavioral Model of 10-kV SiC MOSFET Considering Temperature Effects** **Qian Liu[1], Xiaoyan Tang*[1], Aijun Zhang[1], Yibo Zhang[1], Yushi Liu[1], Yizhen Zhao[1], Yuming Zhang[1]** [1]Xidian University, China

Technical Session 30: Design Methodology & EDA-III

Time	09:00-10:15, October 30, 2026	Venue	Huiyuan Hall
Session Chair	Xingquan Li, Southeast University, China		

Session Details		
09:00	8562	**An Efficient Matrix-Reuse Shooting-Newton Method with Sketched Deflated Restarting GMRES for Periodic Steady-State Analysis** **Nan Zhan[†1], Zhengzhuo Wang[†2], Siyuan Cheng[1], Yunchu Li[2], Zhiwei Li[*1], Jianguo Hu[*2]** [1]South China Normal University, China; [2]Sun Yat-sen University, China
09:15	2198	**Default-Preserving Tuple-Key Repair Scheduling for Open-Source Detailed Routing** **Shengzhi Shen[1+], Wenjun Huang[1+],Yuhe Wang[1+], Zhengzhuo Wang[1], Jiakai Pan[1], Yunchu Li[1],Jianguo Hu[1*]** [1]Sun Yat-sen University, China
09:30	3881	**Graph-Based Extraction of Local Anisotropic Effective Thermal Conductivity from Patterned IC Layouts** **Wangyong Chen, Yufan Qin, Haoyu Zhang, Weizhi Li, Ziyong Wang, Yaojie Mo, Linlin Cai*** Sun Yat-sen University, China; Zhuhai Key Laboratory of Intelligent EDA and Reliability Design of Advanced Integrated Circuits, Zhuhai, China
09:45	5675	**A Liberty-Compatible Aging Variation Modeling Flow for NBTI/HCI-Aware Statistical Timing Signoff** **Guozhu Feng[1,2], Zhengrui Chen[1], Chengjun Guo[1], Shizhang Wang[1], Cheng Zhuo[1*]** [1]Zhejiang University, China; [2]Empyrean Technology, China
10:00	5183	**Design-Aware Guardband Refinement via STA-Guided Selective Library Characterization** **Zhengrui Chen[*], Chengjun Guo, Shizhang Wang** Zhejiang University, China

Technical Session 31: Device Reliability & Security-IV

Time	09:00-10:15, October 30, 2026	Venue	Yaxu Hall
Session Chair	Han Yang, Peking University, China		

Session Details		
09:00	5383	**Modeling Polarity-Asymmetric Threshold-Voltage Drift in SiC MOSFETs under DC Bias Temperature Instability** **Anna Zhang[1], Xin Zhang[1], Li Xiao[1], Rongyao Ma[1], Zhiyu Yang[1], Teng Liu[2],Hanqing Zhao[2], Xuan Li[2,*], Wentong Zhang[2,*], Xiaochuan Deng[2], Bo Zhang[2,*]** [1]China Resources Huajing Microelectronics Co., Ltd., China; [2]University of Electronic Science and Technology of China, China
09:15	2663	**A Low-Capacitance Bidirectional Transient Voltage Suppressor for High-Speed System-Level ESD Protection** **Fengyu Shi[1],Yu Lan[2], Xin Zhang[3], Jinpeng Hao[1], Junke Li[1], Zhao Qi[1*], Ming Qiao[1], Bo Zhang[1]** [1]University of Electronic Science and Technology of China, China; [2]Institute of Sichuan Aerospace Electronic Equipment, China; [3]Chengdu Xinhuo Integrated Circuit Industrial Center Co.Ltd., China
09:30	1504	**A Dual-Node CFET 8T SRAM Compute-in-Memory Cell for Mitigating Direct Heavy-Ion Fault Propagation** **Yiting Ouyang, Linlin Cai*, Zhengxin Zhang, Minghui Dong, Chuhao Chen, Wangyong Chen*** Sun Yat-sen University, China; Zhuhai Key Laboratory of Intelligent EDA and Reliability Design of Advanced Integrated Circuits, Zhuhai, China
09:45	6963	**Comparative Study on Memory Window and Endurance of FeFETs with SiO2/SiN/SiO2 and SiO2/HfO2/SiO2 Gate Interlayers for 3D NAND Applications** **Yajing Ding[1,2], Xiaoyu Ke[1,2], Wenbo Fan[1,2], Runhao Han[1,2], Yuhan Li[1,2], Jia Yang[1,2], JunshuaiChai[1,2], Hao Xu[1,2], Kai Han[3], Xiaolei Wang[12], Wenwu Wang[1,2] and Tianchun Ye[1,2]** [1]Chinese Academy of Sciences, China; [2]University of Chinese Academy of Sciences, China; [3]Weifang University, China
10:00	6360	**Temperature-Dependent Gate Leakage Transport Mechanisms of AlN/GaN MIS-HEMTs With SiN Gate Dielectric** **Bei Xu, Jiejie Zhu, Qin Zhu, Lingjie Qin, Xiaosa Gu,Xiaohua Ma** Xidian University, China

Technical Session 32: Digital Architectures & Systems-III

Time	09:00-10:15, October 30, 2026	Venue	Tianhan Hall
Session Chair	Yang Xu, Zhejiang University		

Session Details		
09:00	2092	**Unified Lightweight Hardware Architecture for Standardized Ascon-Based Cryptographic Schemes** **Shengqi Jiang[1], Wending Huang[1], Yifan Chen[1], Yao Liu[1,2,3,*]** [1]Sun Yat-sen University, China; [2]Fudan University, China; [3]Guangdong Provincial Key Laboratory of Advanced Integrated Circuit Design and Integration Technology, China
09:15	6087	**A Small-Area and Low-Power Softmax Architecture Adapted for Charge-Domain Compute-in-Memory Architectures** **Haobin Li [1,2], Longbin Chen [1,2], Xianping Liu [1,2], Jian Huang*[1,2]** [1]Sun Yat-sen University, China; [2]Guangdong Provincial Key Laboratory of Advanced Integrated Circuit Design and Integration Technology, China
09:30	0039	**A Pipelined FP64 Hardware Accelerator for Next Generation Reservoir Computing** **Yu Meng[1,2], Xiaowen Chen[1,2,*], Liyuan Yang[2], Peisen Li[2], Zhenyu Wu[1], and Hengzhou Yuan[1]** [1]Key Laboratory of Advanced Microprocessor Chips and Systems, China; [2]National University of Defense Technology, China
09:45	1104	**Reconfigurable Hardware Design for Quantized Vector Search** **Bowen P.Y. Kwan[*1], Tim Todman[*2], Ce Guo[*3], Wayne Luk[*4], Jeonghyun Choi[#5], Hyungcheol Noh[#6]** [*]Imperial College London, UK; [#]United Kingdom Seoul, Republic of Korea
10:00	5927	**ZBA-BM: A Configurable Unbiased Approximate Booth Multiplier with Zero-Window Safety** **Haoxuan Li[1], Xiaolei Zhou[1], Zheyu Yan[1,*]** [1]Zhejiang University, China

Technical Session 33: General Analog-IV

Time	10:45-12:00, October 30, 2026	Venue	Qinglian Hall
Session Chair	Weihong Xu, Zhejiang University, China		

Session Details		
10:45	0400	**A 5kHz-BW 77.6-μW 104.7-dB SNDR MES-Free DT Zoom ADC with Active Noise Cancellation** **Yuanhao Zhao[1], Yuke Shen[1,2,*], Jiuhuan Feng[1], Zhong Tang[1], Yanbo Zhang[2], Yuhua Liang[2], Yi Shen[1,2], Shubin Liu[1,2], Ruixue Ding[1,2], Zhangming Zhu[1,2]** [1] Hangzhou Institute of Technology, Xidian University, China; [2] Xidian University, China
11:00	9035	**A 4MHz GaN Buck Converter With Load-Adaptive Negative Gate Bias Control** **Ze Gao[1], Jie Wang[1], Lei Chen[1], Zhenyuan Zhang[1], Xiaoyang Xue[1], Zirui Li[1], Yimeng Zhang[1,2]*, Yuehu Wang[1,2], Yuming Zhang[1,2]** [1] Xidian University, China; [2] Key Laboratory of Analog Integrated Circuits and Systems (Xidian University), Ministry of Education, China
11:15	0093	**A Self-Calibrating Constant-On-Time Control Unit with Capacitance Multiplication for Average Output Current Controlled PFC LED Drivers** **Lufan Chen [1], Yile Xie [1], Ting Yi*[1], Zhiliang Hong [1]** [1] Fudan University, China
11:30	5711	**A Wide-Temperature-Range BGR With Orthogonal Calibration and Hysteresis-Controlled Start-Up** **Jincheng Zhou, Peihe Liu, Yixiao Luo, Li Dang*, Hongzhi Liang, Ruixue Ding and Shubin Liu** Key Laboratory of Analog Integrated Circuits and Systems (Ministry of Education), Xidian University, China
11:45	8731	**A 16-bit 125-MS/s Hybrid Pipelined ADC with a Back-end Time-interleaving Technique** **Zhida Zhang[1], Anji Huang[1,2], Jiuhuan Feng[1], Chunjie Liu[1], Yuke Shen[1,2], Yi Shen*[1,2], Shubin Liu[1,2], Ruixue Ding[1,2], Zhangming Zhu[1,2]** [1] Hangzhou Institute of Technology, Xidian University, China; [2] Xidian University, China

Technical Session 34: CMOS Logic Devices & Sensors-V

Time	10:45-12:00, October 30, 2026	Venue	Huanying Hall
Session Chair	Yang Xu, Zhejiang University		

Session Details		
10:45	8848	**A Data-Efficient AI Framework for Predicting ROSC Performance from Intrinsic Device Characteristics** **Junun Zhu[1]*, Levi Chen[1], Wenhao Wu[1], Yangyang Bao[1], Zhe-Ju Liu[1], Chih-Wei Lin[1], Yi-Chuen Eng[1]*, Chih-Peng Liang[1], Daiki Qin[1], Po-Ju Chen[1], Chia-Yen Li[1], and Jhong-Sheng Wang[1]** [1]Nexchip Semiconductor Corporation, China
11:00	9814	**Width-Dependent Strain Redistribution and Performance Modulation in GAA Nanosheet FETs Revealed by Atomic-Resolution Characterization and TCAD Simulation** **Chao Yan[1], Lan Li[1], Ran Bi [2], Zuoyuan Dong[1], Zhihao Zhang[1], Zhengtao Zhao[1], Xiaomei Li[1], Runsheng Wang[2], Ming Li[2], Xing Wu*[1] and Longda Zhou*[1]** [1] East China Normal University, China; [2] Peking University, China
11:15	7439	**Low Positive Gate Bias Stress-Induced Instability in Amorphous InGaZnO Thin-Film Transistors** **Huan Yang[1], Shengdong Zhang*[1,2]** [1] Peking University, Shenzhen, China; [2] Shenzhen Polytechnic University, China
11:30	0862	**Demonstration of Gate-Last Dual-Sided Vertical FET for Low-Power Logic Applications** **Fangcheng Sun[1,2,#], Yu Liu[2,#], Xinyue He[2], Siyuan Liu[2], Sheng Ye[1], Pengpeng Ren[1], Heng Wu[2,*],Zhigang Ji[1,*]** [1] Shanghai Jiao Tong University, China; [2] Peking University, China
11:45	6756	**CFET with A Novel Post-SD Strategy: Enabling Stress Enhancement and Optimized Interconnect** **Longyu Sun[1], Shiqi Cao[1], Yongliang Li*[1]** [1] State Key Laboratory of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics of the Chinese Academy of Sciences, China

Technical Session 35: Power Devices & Power IC-VI

Time	10:45-12:00, October 30, 2026	Venue	Yuqing Hall
Session Chair	Junji Cheng, University of Electronic Science and Technology of China, China		

Session Details		
10:45	1471	**Design of 1.2 kV-class Enhancement-mode Vertical β-Ga2O3 FinFET with Ultra-low Ron,sp** **Liuyang Dai [1], Xiaorong Zhang *[2], Zhimei Yang *[1], Mingmin Huang [1], Min Gong [1], Yao Ma [1], Yun Li [1]** [1] Sichuan University, China; [2] China Resources Microelectronics Ltd., China
11:00	3156	**Recovery Behavior of Electron-Irradiated SiC MOSFETs by Repetitive Short-Circuit Stress** **Peilin Chen[1,2], Huanshi Guo[1], Ganquan H[1], Mingmin Huang*[1], Xin Zhang*[2,3], Yao Ma[1], Zhimei Yang[1], Yun Li[1]** [1] Sichuan University, China; [2] Wuxi China Resources Huajing Microelectronics Company Ltd, China; [3] Fudan University, China
11:15	5714	**A SiC Lateral MOSFET Paralleled with Schottky Barrier Diode for Low Reverse Recovery Charge** **Chenyang Wan[1], Wenhao Yang[1], Yaqi Xu[1], Xian Xue[1], Yimeng Zhang*[1], Yuming Zhang[1]** [1] Xidian University, China
11:30	8679	**A 4H-SiC LDMOS for Wide-range Temperature Application with Stable Threshold Voltage** **Yaqi Xue[1], WenHao Yang[1], ChenYang Wan[1], Xian Xue[1], Yimeng Zhang*[1], Yuming Zhang[1]** [1] Xidian University, China
11:45	2835	**High-Voltage β-Ga2O3 MOSFET With Striped P-NiO Hetero-source-field-plate** **Jie Wei *[1], Yongcheng Gao[1], Jialei Tan[1], Xiangnan Li[1], Yuxi Wei[1], Bo Zhang[1], and Xiaorong Luo[1,2]** [1] University of Electronic Science and Technology of China, China; [2] Chengdu University of Information Technology, China

Technical Session 36: Design Methodology & EDA-IV

Time	10:45-12:00, October 30, 2026	Venue	Huiyuan Hall
Session Chair	Xingquan Li, Southeast University, China		

Session Details		
10:45	7033	**MSG-GAN: Enabling Constrained Test Pattern Generation for Integrated Circuits Advanced Manufacturing** **Yuqin Wang[†,1,2], Tianyang Gai[†], Yajuan Su[*,1,2], Xiaojing Su[1,2], Pengyu Ren[1,2], Yujie Jiang[1,2],Zhanzi Chen[1,2], Tianao Chen[1,2] and Yayi Wei[*,1,2]** [1]Chinese Academy of Sciences, China; [2] University of Chinese Academy of Sciences, China
11:00	8134	**AI-Assisted Specification-to-Layout Generation and Silicon Verification of 25V HVMOS Devices** **Hayato Wang[1#*], RR Zhu[1#*], Levi Chen[1], Yi-Chuen Eng[1*], Chih-Peng Liang[1], Chih-Wei Lin[1], Po-Ju Chen[1], Daiki Qin[1], Zhe-Ju Liu[1], Jhong-Sheng Wang[1], and Chia-Yen Li[1]** [1] Nexchip Semiconductor Corporation, China
11:15	2116	**AL-CNNCap: Active-Learning-Enabled Training for CNN-Based Capacitance Extraction of Interconnects** **Xin Sun[1], Jiechen Huang[2], Wenjian Yu[2*]** [1] Qinghai University, China; [2] Tsinghua University, China
11:30	2192	**A Unified SOT-MRAM Model for Synergistic In-Plane and Perpendicular Anisotropy** **Chenyi Wang[1,2,†], Xiaoyang Xu[1,2,†], Chao Wang[1,*], Zhaohao Wang[1,2,3]** [1]Hangzhou International Innovation Institute, Beihang University, Hangzhou, China; [2]Beihang University, China; [3]Shandong Laboratory of ASIC and Intelligent Instruments in Qingdao, Beihang University, Qingdao, China
11:45	1707	**Blockage-Aware Hotspot-Driven On-Chip Monitor Placement via Weighted Voronoi Optimization** **Yizhe Chen[1], Wenyong Zhou[*2], Yuannuo Feng[1], Wenshuai Yao[4], Chenxi Hu[3], and Wang Kang[*1]** [1] Beihang University, China; [2] The University of Hong Kong, Hong Kong, China; [3] The Hang Seng University of Hong Kong, China; [4] Peking University, China

Technical Session 37: Device Reliability & Security-V

Time	10:45-12:00, October 30, 2026	Venue	Yaxu Hall
Session Chair	Yixu Yao, Institute of Microelectronics of the Chinese Academy of Sciences, China		

Session Details

10:45	3381	**Profiling Cross-Sectional Trap Distribution in FinFETs Channel Under Hot-Carrier Stress** **Mingyang Sun[1,2], Qianqian Liu[2,4], Qingyuan Li[2,3], Qingzhu Zhang[1,2,3], Huaxiang Yin[1,2,3], XiaoleiWang[1,2,3], Jun Luo[1,2,3], Hong Yang*[1,2,3]** [1] University of Chinese Academy of Sciences, China; [2] Chinese Academy of Sciences, China; [3] University of Chinese Academy of Sciences, China
11:00	6677	**A Ratio-Based RC Temperature Sensor with Common-Mode Cancellation and Aging-Resilient Architecture** **Yuduan Cao, Xiaochang Zhang, Yongqiang Zhong, Hongbei Jin, Huizhen Qiu, Pengpeng Ren* and Zhigang Ji** Shanghai Jiao Tong University, China
11:15	3410	**Reliability Assessment of GaN Tunneling Hot Electron Transistors** **Weiyu Ren[1], Zhijie Chang[1], Ling Yang*[1], Xu Zou[1], Xiaohua Ma[1], and Yue Hao[1]** [1] Xidian University, China
11:30	4642	**Image Analysis of Fin Geometry Variation at the Atomistic Scale** **Chen Shen[1], Zuoyuan Dong[1, 2], Xing Wu*** [1] East China Normal University, China; [2] Peking University, China
11:45	5031	**HR2-PUF: An RRAM Strong PUF Resilient to Machine-Learning and Structure-Aware Annealing Attacks for Robust Hardware Authentication** **Houcheng Liu[1], Zongwei Wang*[1,2], Borui Shi, Lin Bao, Ling Liang, Yimao Cai[1]** [1] Peking University, China; [2] YanXin Micro Electronics Co., Ltd. (YXME), China

Technical Session 38: Power Devices & Power IC-VII

Time	10:45-12:00, October 30, 2026	Venue	Shuibo Hall
Session Chair	Kemeng Yang, Nanjing University of Posts and Telecommunications, China		

Session Details		
10:45	6642	**A GaN Half-Bridge Gate Driver with Self-Regulated Three-Level Gate Biasing and State-Retentive Level Shifter** **Yifei Zheng[1], Qing Yuan[2], Bowen Xue[1], Qianheng Dong[1], Jing Zhu[*3], Long Zhang[1], Weifeng Sun[*1]** [1] Southeast University, Nanjing, China; [2] Fudan University, China; [3] Chipfavor Semiconductor Co., Ltd., China
11:00	4138	**Enhanced Unclamped Inductive Switching Ruggedness for GaN HEMT by Hybrid Power Switch** **Gang Xue[1], Gaoqiang Deng[1*], Zijun Wei[1], Lian Zhang[2], Bo Zhang[1], and Xiaorong Luo[1,2,3*]** [1] University of Electronic Science and Technology of China, China; [2] Chengdu University of Information Technology, China; [3] University of Electronic Science and Technology of China, China
11:15	7766	**Impact of SBR Gate Oxide Thickness and Ratio on the Performance of SGT-SBR Integrated Devices** **Xuan Xiao[1, 2#], Jun Ye[2#], Ruihan Gao[3#], Yufei Xiong[2], Weiye Mo[2], Lei Jin[2], Jiafeng Xie[2], Yang Song[2], Yao Ma[1], Naijie Zhang[2], Min Gong[*1], Mingmin Huang[*1], Wei Huang[*4]** [1] Sichuan University, China; [2] China Resources Microelectronics (Chongqing) Co., Ltd., China; [3] Fudan University, China; [4] Jiangnan University, China
11:30	9882	**A High Power Density Quartet-Phase Isolated DC-DC Converter Using Wide Bandwidth V-F-V Isolated Amplifier** **Jiahui Liu[1], Xiaoying Chen[1], Guanzhi Chen[1], Shizhe Ren[1], Shaowei Zhen*[1], Zuyue Pang[1], Yining Yang[1], Yourun Zhang[1], Yanliang Li[2], Jia-Ning Zhang[2], Yikang Li[2], Bo Zhang[1]** [1] University of Electronic Science and Technology of China, China; [2] Chongqing Optoelectronics Research Institute, China
11:45	6754	**Design and Implementation of Total Ionizing Dose Hardening for A 30 V LDMOS Based on 110 nm BCD Technology** **Yanfei Li[1,2,3], Jialin Sun[2,3], Xuecheng Jiang[2,3], Enci Lin[2,3], Ming Qiao*[1], Bing Ding[2,3], Rubin Xie[1,2,3],Genshen Hong[2,3], Shaoli Zhu[2], and Bo Zhang[1]** [1] University of Electronic Science and Technology of China, China; [2] The 58th Research Institute of China Electronics Technology Group Corporation, China; [3] National Key Laboratory of Integrated Circuits and Microsystems, China

Technical Session 39: RF & Wireless-III

Time	10:45-12:00, October 30, 2026	Venue	Tianhan Hall
Session Chair	Kai Tang, Hunan University, China		

Session Details

10:45	3883	**A 15–25 GHz 2.8 dB NF Transformer-Based LNA With Gm-Boosting in 28 nm CMOS** **Liwei Zhao, Peiqi Jin, Qiang Guo, Yi Tang, and Zhe Liu** Tianjin University, China
11:00	4106	**Thin-barrier AlGaN/GaN HEMTs on 6-inch Silicon with 0.8 dB Noise Figure and 14.9 dB Associated Gain for Low-Voltage Applications** **Gaopeng Huang[1,*], Jiejie Zhu[1,*], Yifan Chen[1], Mengdi Li[1], Lai Meng[1], Xiaohua Ma[1], Yue Hao[1]** [1] Xidian University, China
11:15	4713	**A 5 GS/s 8-bit Time-Domain ADC Featuring a Capacitor-Discharging Time Amplifier** **Xuan Luo[1,2], Chuanshi Yang*[2], Xijun Huang[1], Kai Tang*[1], Yuanjin Zheng[3], Hao Gao[2]** [1] Hunan University, China; [2] Southeast University, China; [3] Nanyang Technological University, Singapore
11:30	1915	**A 133 GHz 13.6 mW Distributed Voltage Controlled Oscillator with Transistor-Induced Tunability** **Henrique Iha Taguti, Yann Deval, Hervé Lapuyade, Magali De Matos, Marina Studniarek, François Rivet** University Bordeaux, France
11:45	7837	**A Low-Spur Charge-Pump PLL With Random Chopping and Offset Compensation** **Junhao Yang[1], Sheng Wang[1], Chao Yang*[1], Jing Jin[1]** [1] Shanghai Jiao Tong University, China

Technical Session 40: General Analog-V

Time	13:30-15:30, October 30, 2026	Venue	Qinglian Hall
Session Chair	Yibo Qiao, Zhejiang University, China		

Session Details		
13:30	7917	**A Three-Channel Low-Noise Wideband Transimpedance Amplifier for Fiber Optic Gyroscopes** **Zelin Li[1,2], Tao Yin[1,2]*, Zhicheng Sun[3], Jian Liu[1,2], Nanjian Wu[1,2], Liyuan Liu[1,2]** [1] University of Chinese Academy of Sciences, China; [2] Chinese Academy of Sciences, China; [3] Yunnan Normal University, China
13:45	8600	**A Dual-Phase Adaptive-On-Time Buck Converter with PLL-Based Phase Interleaving and Active Current Balancing** **Zicong Liu[1,2], Yongxiang Weng[3], Wanyuan Qu*[1]** [1] Zhejiang University, China; [2] Polytechnic Institute of Zhejiang University, China; [3] The 51st Research Institute of China Electronics Technology Group Corporation, China
14:00	4411	**A Timing-Efficient Noise-Decoupled FIR-Pipe-SAR ADC for Low-Power Receivers** **Jintian Li[1], Qiang Li[2], Jinhang Sun[1], Yu Lu[1], Junyu Wang[1] and Hao Min*[1,2]** [1] Fudan University, China; [2] Shanghai Quanray Electronics Co., Ltd. China
14:15	0190	**A 15-bit 500 kS/s Two-stage Pipeline-SAR ADC with Bit Weight Background Calibration** **Beichen Zhao[1, †], Shuangyu Lyu[1, †], Yixiao Hu[1], Jian Mei[1,2], Ting Yi*[1]** [1] Fudan University, China; [2] National Integrated Circuit Innovation Center, China
14:30	0798	**A FVF Based Capacitor-less LDO with Wideband High PSR** **Runzhang Wang*[1], Zhentao Yang [1], Linjie Liu [1]** [1] The 13th research institute, CETC, China
14:45	2087	**A 1-GS/s 12-bit SAR-Assisted Pipelined ADC With a Hybrid-Supply Ring Amplifier** **Houhu Cui, Fan Ye*** Fudan University, China
15:00	8407	**A 11-bit 400 MS/s Pipelined-SAR ADC Using Correlated Level Shifting and Passive Residue Transfer** **Zhipeng Feng, Yunchu Li*** Sun Yat-sen University, China
15:15	4512	**A Low-Power Bandpass-Filtering Listening Wake-Up Circuit** **Shengsheng He*[1], Zhengjie Li[1], Zehong Li*[1]** [1] University of Electronic Science and Technology of China, China

Technical Session 41: CMOS Logic Devices & Sensors-VI

Time	13:30-15:30, October 30, 2026	Venue	Huanying Hall
Session Chair	Zeheng Wang, Xidian University, China		

Session Details		
13:30	5569	**Process Thermal Budget Optimized Vertical Gate-All-Around FETs with In-situ Doped SiGe/Si/SiGe Nanosheets and HfO2/TiN HKMG** **Xijun Zhou[1], Ran Bi[1], Shunli Xu[1], Jianhuan Wang[4], Chenyao Huang[1], Haoran Zhao[1], Yifan Chen[1], Xiaoyan Xu[1,2], Xia An[1,2], Heng Wu[1,2], Jianjun Zhang*[3], and Ming Li*[1,2]** [1] Peking University, China; [2] Beijing Advanced Innovation Center for Integrated Circuits, China; [3] Chinese Academy of Sciences, China; [4] Beijing Academy of Quantum Information Sciences, China
13:45	3337	**High Performance and Thermally Stable Quasi-Ohmic Contacts in Scaled IGZO Vertical FETs by Oxygen Vacancy Engineering** **Meichen Jin*†, Chang Liu†, Zhengyong Zhu*, Jing Liang, Jiabao Sun, Wei Yu, Fuwang Yang, ShujuanMao, Chao Tian, Hongbo Sun, Jing Zhang, Guilei Wang, Bok-Moon Kang, Chao Zhao** Beijing Superstring Academy of Memory Technology, China
14:00	7270	**Controllable Construction of Realistic GAAFET Models at Atomic Level** **Wen-Feng Li[1,2], Zheng-Neng Zheng[2], Lin-Wang Wang[2], Zheng-Mei Yang[1]*, Yue-Yang Liu[2]*** [1] Beijing University of Posts and Telecommunications, China; [2] Chinese Academy of Sciences, China
14:15	0713	**Enhancing the Performance of Ultrathin ALD-IGO TFTs via Synergistic Interface Engineering** **Xian Cai[1], Juyu Li[1], Shengjie Yang[1], Huan Yang[1], Lei Lu[1], Shengdong Zhang*[1,2]** [1] Peking University, Shenzhen, China; [2] Shenzhen Polytechnic University, China
14:30	4066	**A Parallel Addressable Resistance Test Circuit for Yield Enhancement in Advanced Technology Nodes** **Huizhen Qiu[1], Yewei Zhang[2], Pengpeng Ren*[2], Zhiguo Yu[1], Zhigang Ji[2] and Xiaofeng Gu*[1]** [1] Jiangnan University, China; [2] Shanghai Jiao Tong University, China
14:45	9189	**Topology-Aware Thermal Modeling of Sequential CFET Standard Cells** **Taoyu Zhou[1], Naiqi Liu[1], Yandong He[1], Gang Du[1,2,*]** [1] Peking University, China; [2] Beijing Innovation Center of Integrated Circuits, China
15:00	4487	**Circuit-Level Performance Evaluation and Co- Optimization of Sub-1-nm GAA CNT FETs** **Botong Zhao[1], Baoyi Min[1], Peng Liu[1], Chunxin Li[1], Hua Qiang[1], Jiahao Wang[1], Bingyi Ye[1], Yuhang Zhang[1], Xiaojin Li[1], Yang Shen*[1], Yabin Sun*[1]** [1] East China Normal University, China
15:15	4396	**Self-Consistent Poisson–Schrodinger Comparison of Pseudomorphic GaAs-Based and Lattice-Matched InP-Based InxGa1−xAs HEMT Platforms**

		Chengyi Li[1], Anika Tasnim[2], Jinjin Jiang[1], Aynul Islam[1,3,*] [1] University of Electronic Science and Technology of China, China; [2] University College London, United Kingdom; [3] University of Glasgow, United Kingdom

Technical Session 42: Power Devices & Power IC-VIII

Time	13:30-15:30, October 30, 2026	Venue	Yuqing Hall
Session Chair	Yawei Chen, CRMicro, China		

Session Details		
13:30	3081	**Thermally Adaptive SOI-LDMOS with Ultra-Low Ron,sp and Mitigated High-Temperature Degradation** **Zhuoxian Cai[1], Teng Liu[1,2], Yujing Fu[1], Jingchuan Zhao[2], Zhili Zhang[2], Hua Song[2], Lin Bai[2], XinyuWang[2], Nailong He[2], Sen Zhang[2], Wentong Zhang[1*], Zhaoji Li[1] and Bo Zhang[1]** [1] University of Electronic Science and Technology of China, China; [2] CSMC Technologies Corporation, China
13:45	4733	**A Quasi-Superjunction PMOS with Low VTH for Monolithic High-Voltage 4H-SiC Integrated Circuits** **Jiang Xu[1], Yiqi Chen[1], Tianchun Nie[1], Mengyao Zhao[1], Qinsong Qian[1,2], Yu Huang[3], Runhua Huang[3], Song Bai[3], Siyang Liu[1], Weifeng Sun[1], Jie Ma*[1], Long Zhang*[1]** [1] Southeast University, China; [2] Research Institute of Application Specific Integrated Circuits Matched organization Jiangsu Industrial Technology Research Institute, China; [3] Nanjing Electronic Device Institute, China
14:00	8585	**A Symmetric Cu Clip Top-Side Commutation SiC Power Module with Low Parasitic Inductance and Improved Current Sharing Performance** **Xiaona Zhang[1], Zihao Chen[1], Qingqi Lin[1], Lejia Sun*[1,2], Yuming Zhang[1,2]** [1] Xidian University, China; [2] Key Laboratory of Wide Band-Gap Semiconductor Materials and Devices, China
14:15	0182	**A Novel Ultra-low Specific On-resistance 40V LDMOS with Split Slant Field Plate Fabricated via Multi-step Etching** **Teng Liu[1,2], Yongsheng Sun[3], Rongshuo Liu[1], Yongshun Li[1,2], Hao Wang[2], Yiduo Xie[2], Longhui Lin[2],Yueyu Zhang[1], Shengyuan Wang[1], Huajun Jin[2], Liang Song[2], Nailong He[2], Dejing Wang, Sen Zhang[2],Hao Fang[3], Wentong Zhang[1*] and Bo Zhang[1*]** [1]University of Electronic Science and Technology of China, China; [2] CSMC Technologies Corporation, China; [3] Wuxi China Resources Microelectronics Co., Ltd., China
14:30	9896	**A Phase-Scalable Capacitive-Bus Hybrid Buck Converter for High Current xPU Applications** **Chenguang Lv[1], Shaowei Zhen*[1], Zuyue Pang[1], Lixing Wang[1], Yongsheng Du[2], Yining Yang[1], Haokang Lin[2], Xiaowen Chen[3], Chang Liu[3], Bo Zhang[1]** [1] University of Electronic Science and Technology of China, China; [2] Chengdu Enjixin Technology Co., Ltd., China; [3] National University of Defense Technology, China

14:45	0223	**Influence of LOCOS Width on Radiation Hardening Characteristics of Power MOSFETs** **Hu Jin[1], YaBin Sun[1], Chenchen Zhang[2], Xin Wan[3]** [1] East China Normal University, China; [2] Yangtze Delta Region Institute of Tsinghua University, China; [3] Hangzhou Aurorachip Semiconductor Co., Ltd., China
15:00	0280	**Electron-Irradiation-Induced Degradation of 40 V Shielded-Gate Trench MOSFETs** **Kelin Yuan[1,2], Mingmin Huang[1*], Ling Song[2*], Xuan Xiao[1,3], Ailin Qiu[1], Yao Ma[1], Zhimei Yang[1]** [1] Sichuan University, China; [2] China Resources Microelectronics Company Ltd., China; 3 China Resources Microelectronics (Chongqing) Co., Ltd., China
15:15	4529	**Surrogate-Navigated and TCAD-Anchored Multi-Objective Field-Limiting Ring Design for 1200-V Super-Junction MOSFETs** **Guanxi Chen[†], Han Guo[†], Zhihang Hou, Zhiwei Jing, Mengxi Liu, Haimeng Huang[*]** University of Electronic Science and Technology of China, China

Technical Session 43: Design Methodology & EDA-V

Time	13:30-15:30, October 30, 2026	Venue	Huiyuan Hall
Session Chair	Pengying Chang, Beijing University of Technology, China		

Session Details		
13:30	4852	**A Self-Consistent Transport Model for Two-Dimensional Ferroelectric Tunnel Junction with Metal-Ferroelectric-Insulator-Graphene Structure** **Enshu Xu, Guowei Ma, Wenkai Li, Yongchang Chi, Pengying Chang*** Beijing University of Technology, China
13:45	2967	**PEER: Pattern-Embedded Expert Router with Layout Knowledge for Fast Standard-Cell Routing** **Dongpei Liu, Yufan Ren, Zhien Li, Zhenyu Zhao*** National University of Defense Technology, China
14:00	1740	**Accurate Analytical 3D Fringe Capacitance Modeling for M0-Integrated n-type 3fin FinFETs** **Jianchang Lu[1,2], Rongsheng Chen[*1,2], Bing Lu[*3]** [1] South China University of Technology, China; [2] The Engineering Research Center of Design and Technology Co-Optimization of Integrated Circuits, Ministry of Education, China; [3] Primarius Technologies Co., Ltd., China
14:15	0184	**Reinforcement Learning-Based Neighborhood Search for Cost-Effective Chiplet Decomposition** **Yaofu Sun, Xiaopeng Li, Yi Yang, Dongzhu Gao, Yu Gong*** Nanjing University of Aeronautics and Astronautics, China
14:30	1701	**Unified Modeling of IGZTO TFT Electrical Characteristics Based on Physical Model and Neural Network Fusion** **Jialong Tang[1,†], Shuanggui Liu[1,†], Yiming Jia[1], Kai Chen[1,2], Yang Xu[1,2,3], and Yunlong Li[1,2,3,*]**

		[1] Zhejiang University, Hangzhou, China; [2] Zhejiang ICsprout Semiconductor Co., Ltd, China; [3] Zhejiang University, China
14:45	6366	**An Instruction-Level Power Modeling Method with Hotspot Analysis for RISC-V Processors** **Chaofan Huang[1], Xuefei Ming[2], Shuli Liu[2], Jianfei Jiang*[1]** [1] Shanghai Jiao Tong University, China; [2] The 58th Research Institute of China Electronics Technology Group Corporation, China
15:00	0663	**ValTrace: Boundary-Scoped Validation Memory for Analog Layout Candidates** **YUHE WANG[1,†], SHENGZHI SHEN[1,†], WENJUN HUANG[1,†], ZHENGZHUO WANG[1], JIAKAI PAN[1], YUNCHU LI[1], YUXUAN HUANG*[,3], JIANGUO HU*[,1,2]** [1] Sun Yat-sen University, China; [2] Shenzhen Research Institute of Sun Yat-sen University, China; [3] Guilin University of Electronic Technology, China
15:15	9613	**A Simplified Dual-Input Memory Polynomial Model for Power Amplifiers under Load Mismatch** **Jimin Wen*, Jinxin Zhang*, and Jun Tao†** *Xpeedic Co., Ltd., China; † Fudan University, China

Technical Session 44: Device Reliability & Security-VI

Time	13:30-15:30, October 30, 2026
Venue	Yaxu Hall
Session Chair	Chaoyue Zheng, Yangtze Delta Region Institute (Huzhou), University of Electronic Science and Technology of China, Huzhou, China

Session Details

13:30	2353	**Trap-Resolved Pulse-IV Characterization Enables Reliability-Driven CMOS Process Optimization** **Yanlin Yao[1], Danfu Xu[2], Weiwei Gou[3], Shiqi Liu[3], Haiting Li[3], Xiaoxia Fan[4], Pengpeng Ren[1], and Zhigang Ji[1,*]** [1] Shanghai Jiao Tong University, China; [2]Shanghai Huaxinji Technology Corporation, China; [3] Maxscend Corporation, China; [4] Keysight Technologies Corporation, China
13:45	6294	**Impact of Interface and SiC-Side Traps on Threshold Voltage Drift in Aged SiC MOSFETs under Repetitive Short-Circuit Stress** **Ze Zhao[1], Hanqing Zhao[1], Mingyang Li[1], Cheng Yang[1], Jiahao Hu[1], Yuewei Guo[2], Lei Duan[2], Jiaqi Zhang[2], Xuan Li*[1], Bo Zhang[1]** [1] University of Electronic Science and Technology of China, China; [2] Hebei Bowei Integrated Circuits Co., Ltd., China
14:00	9493	**Hardware and Data Co Design for SiC MOSFET Gate Oxide Aging Monitoring and Bayesian Remaining Useful Lifetime Prediction** **Lintao Shi[1], Song Qiu[1,*], Fengda Cheng[1], Kai Ou[1]** [1] Southwest Jiaotong University, China
14:15	0366	**A Novel Concept, Framework and Model of ESD Testing System for Latch-Up Evaluation** **Junke Li[1], Yu Lan[2], Xin Zhang[3], Fengyu Shi[1], Jinpeng Hao[1], Zhao Qi[1*], Ming Qiao[1], Bo Zhang[1]**

		[1] University of Electronic Science and Technology of China, China; [2] Institute of Sichuan Aerospace Electronic Equipment, China; [3] Chengdu Xinhuo Integrated Circuit Industrial Center Co. Ltd, China
14:30	2684	**Non-Profiled Side-Channel Attack on Multi-Tenant FPGAs via Regularized DDLA with Binary Classification** **Shenyong Mao, Yankun Zhu, Pingqiang Zhou** ShanghaiTech University, China
14:45	4431	**Off-State Stress Degradation Mechanism for AlN/GaN MIS-HEMTs on Si Substrates** **Bei Xu, Jiejie Zhu, Qin Zhu, Lingjie Qin, Xiaosa Gu,Xiaohua Ma** Xidian University, China
15:00	9853	**Reliability Characteristics of 650-V VD-MOSFETs Passivated with Silicon-Rich Nitride/Polyimide** **Lin Yin[a,b], Jiatai Peng[a], Chuanqi Ni[a], Xingzheng Hu[a,b], Zhenhua Hu[b], Xiaoyu Liu[a], Kehao Zhang[b],Huanhuan Yang[b], and Xi Tang[a,*]** [a] Anhui University, China; [b] Chuzhou HRM Electronic Technology Co., Ltd, China
15:15	9344	**On-State Electrical Stability of Flexible Lateral Drift Region Organic Field-Effect Transistors under Mechanical Bending Stress** **Hengdian Chang, Jun Zhang, Qiushi Zhang, Haonan Lin, Meng Xie, Jiafei Yao, Kemeng Yang, Jing Chen, Man Li, Yufeng Guo*** Nanjing University of Posts and Telecommunications, China

Technical Session 45: Power Devices & Power IC-IX

Time	13:30-15:30, October 30, 2026	Venue	Shuibo Hall
Session Chair	Xin Zhou, University of Electronic Science and Technology of China, China		

Session Details

13:30	0833	**Total-Ionizing-Dose Effects for GaN-on-Si Power HEMTs with Floating Substrate Termination** **Xintong Xie[1], Shuxiang Sun[2], Pengfei Zhang[1], Gaoqiang Deng[1*], Bo Zhang[1], and Xiaorong Luo[1,3,4*]** [1] University of Electronic Science and Technology of China, China; [2] Huanghuai University, China; [3] Chengdu University of Information Technology, China; [4] University of Electronic Science and Technology of China, China
13:45	1643	**Thin AlGaN-Barrier p-GaN HEMTs with Enhanced Short-Circuit Robustness via Self-Adaptive Protection** **Ning Yang[1], Binju Qiu[1], Yunxiang Xing[1], Jilin Yang[1], Jinggui Zhou[1], Jianggen Zhu[1], David Zhou[2]*,Danfeng Mao[2], Chao Feng[2], Bo Zhang[1] and, Qi Zhou[1,3,4]*** [1] University of Electronic Science and Technology of China, China; [2] Shenzhen Pinghu Laboratory, China; [3] Shenzhen Institute for advanced study of UESTC in Shenzhen, China; [4] Institute of Electronic and Information Engineering of UESTC in Guangdong, China

14:00	9741	**Al2O3-Capped HfO2 Gate Stack for Improved High-Field Reliability in β-Ga2O3 Power MOSFETs** **Chunxiao Yu[1], Xiang Zheng*[2], Jun Zheng[3], Yan Liu[1], Yue Hao[1], and Genquan Han*[1,2]** [1] Xidian University, China; [2] Hangzhou Institute of Technology, Xidian University, China; [3] Institute of Semiconductors, Chinese Academy of Sciences, China
14:15	7291	**Multiphysics Analysis of a Novel Co-Packaging GaN/SiC Cascode Device** **Ying Dai, Xiaoping Wang, Haizhao Zhi, Xinpeng Lin, Jinghan Xu, Sirui Feng*** Shenzhen Pinghu Laboratory, China
14:30	0926	**Three-Dimensional Variational Vertical Doping Superjunction Device** **Yuxiang Pang[1], Zhentao Xiao[1], Chenxing Wang[2], Fuxian Zhang[3], and Haimeng Huang[1,3,†]** [1] Glasgow College, University of Electronic Science and Technology of China, China; [2] University of California, USA; [3] University of Electronic Science and Technology of China, China
14:45	1438	**A Novel SiC JBS Diode with Locally Heavily Doped Floating Island Structure for Low Dynamic On-resistance Degradation** **Zijing Yue, Jiafei Yao*, Ziwei Hu, Wenyong Wang, Qi Sun, Jing Chen, Man Li, Kemeng Yang, Wentong Zhang, Yufeng Guo*** Nanjing University of Posts and Telecommunications, China
15:00	6684	**4H-SiC Double-Trench MOSFET with Integrated MOS-Channel Diode and Split Source Trench** **Boyu Huang[1], Yihong Liang[1], Xinwei Song[1], Maojiu Luo[2], Bo Zhang[1], Yourun Zhang*[1]** [1] University of Electronic Science and Technology of China, China; [2] Gree Electric Applicances, Inc., China
15:15	6625	**GaN Back-Gate p-Channel Transistors with Enhanced Current Density** **Jialin Duan[1#], Teng Li[1#], Sihang Liu[1], Yunhong Lao[1], Jingjing Yu[1], Junjie Yang[1], Han Yang[1],Maojun Wang[1], Yang Liu[2], Jinyan Wang[1], and Jin Wei*[1]** [1] Peking University, China; [2] Sun Yat-Sen University, China

Technical Session 46: RF & Wireless-IV

Time	13:30-15:30, October 30, 2026	Venue	Tianhan Hall
Session Chair	Remi Queheille, University of Bordeaux, France		

Session Details

13:30	5558	**A 7.5-to-9.1GHz Highly Reliable Differential Series-Resonance Oscillator Achieving-130.8 dBc/Hz PN at 1MHz Offset** **Ke Sun, Ang Hu*, Dongsheng Liu, Jiahao Lu** Huazhong University of Science and Technology, China

13:45	0728	**High-Gain Vertical GaN Hot-Electron Transistors Enabled by Graded Barrier and Ultra-Thin Base Polarization Engineering** **Zhijie Chang, Weiyu Ren, Ling Yang*, Tao Lv, Xiaohua Ma, and Yue Hao** Xidian University, China
14:00	5437	**A 10b 500MS/s Subranging SAR ADC with Splittail-current-source Low-noise Comparator and ETDAS in 28nm CMOS** **Shupei Yang[1,2], Bifei Wang[1,2], Kai Sun[1], Hanbo Jia[1], Ming Chen[1], Xuan Guo*[1]** [1] Institute of Microelectronics of the Chinese Academy of Sciences, China; [2] University of Chinese Academy of Sciences, China
14:15	9865	**The Effect of Channel Thickness on the Noise Performance of Thin-barrier AlGaN/GaN HEMTs** **Gaopeng Huang *, Jiejie Zhu *, Yifan Chen, Mengdi Li, Lai Meng, Xiaohua Ma, Yue Hao** Xidian University, China
14:30	1072	**Design of an Equal Three-way Wilkinson Power Divider in GaAs pHEMT Technology with High Phase Consistency** **Jiachen Qian[1], Rubing Han[2], Hualong Ji[1], Hui Chen[3], Yan Jiang*[1]** [1] Nanjing University of Posts and Telecommunications, China; [2] Shanghai Radio Equipment Research Institute, China; [3] Nanjing University of Aeronautics and Astronautics, China
14:45	2417	**A Fast-Locking Bang-Bang PLL Based on Two-Point Frequency Search and Type-II Gear-Shifting Technique** **Xichen Zhu[1], Sheng Wang[1], Chao Yang*[1,2], Jing Jin[1,2]** [1] Shanghai Jiao Tong University, China; [2] Ministry of Education's Advanced Interface IP Engineering Research Center, Shanghai Jiao Tong University, China
15:00	2028	**A 28-nm CMOS Wideband High-Linearity Digitally Controlled Variable-Gain Output Driver for Direct-RF DACs** **Hua Zhang, Jianguo Hu*, Yunchu Li** Sun Yat-sen University, China
15:15	1905	**A 23–29 GHz CMOS Power Amplifier with Transistor-Based Capacitive Neutralization** **Jiu Peng[1], Yang Chen*[1], Qiangji Wang[1], Yuzhao Wen[1], Bo Yan[1]** [1] University of Electronic Science and Technology of China, China

Technical Session 47: Power Devices & Power IC-X

Time	16:00-17:45, October 30, 2026	Venue	Guofeng Hall I
Session Chair	Yawei Chen, CRMicro, China		

Session Details

16:00	1983	**A 20-MHz Buck Converter with Comparator-Delay Adaptive Modulation Control** **Shihao Xiao [1], Bin Yang [1], Xufeng Liao[1,2] and Lianxi Liu*[1,2]** [1] Xidian University, China; [2] Xidian University Chongqing ICs Innovation Institute, Xiyong Microelectronics Park, China

16:15	3192	**A 2-MHz Digitally Controlled Buck Converter With Noise-Shaping SAR Feedback for Low Ripple and Fast Transient Response** **Zihan Zheng[1,2], Shuyan Zhu[1,2]*, Qinwei Lai[3], Shaolin Liao[4], Yunchu Li[1,2]** [1] Sun Yat-sen University, Zhuhai, China; [2] Zhuhai Key Laboratory of Millimeter-wave Terahertz Antenna and RFIC, SYSU, China; [3] AMICRO Semiconductor Co., Ltd., China; [4] Sun Yat-sen University, China
16:30	6387	**A Multi-Voltage Domain Power Management Unit with Dynamic Voltage Scaling for DSP** **Tianyi He[1], Ping Luo*[1], Jingnan Ren[1], Zhibing Li[1], Hao Wang[1], Shaowei Zhen[1], Chang Liu[2], Xiaowen Chen[2]** [1] University of Electronic Science and Technology of China, China; [2] National University of Defense Technology, China
16:45	7047	**A Novel Vertical Superjunction GaN MOSFET with Ultra-Low Specific On-Resistance and Reverse Recovery Loss** **Heming Yin, Yue Zou, Xuerui Shi, Qizhi Feng, Jiaxin Li, Bo Yi, and Moufu Kong*** University of Electronic Science and Technology of China, China
17:00	6026	**A 94.1% Peak-Efficiency Low-Power Tri-Mode Boost Converter with Frequency Feedback Loop** **Zihang Guo[1,2], Yimeng Zhang*[1,2], Wei Zhou[1,2], Yuming Zhang[1,2]** [1] Xidian University, China; [2] Key Laboratory of Analog Integrated Circuits and Systems (Xidian University), Ministry of Education, China
17:15	5797	**Novel Enhancement-Mode Lateral β-Ga2O3 MOSFET with High Power Figure of Merit** **Yuxi Wei[1], Yan Wang[1], Heng Sun[1], Zejun Jiang[1], Jie Wei[1,*], and Xiaorong Luo[1,2]** [1] University of Electronic Science and Technology of China, China; [2] Chengdu University of Information Technology Chengdu, China
17:30	2204	**Machine Learning Modelling and Multiobjective Process Window Optimization for Power VDMOS Devices** **Lei Huang[a], Xingzheng Hu[b], Xiaoyue Ding[c], Lin Yin[b], Lu Xue[b], Yue Zhao[a], Zhiming Tian[d], Kun Wu[d],Wenping Cao[a], Cungang Hu[a], Zhaofu Zhang[c,*], and Xi Tang[a,*]** [a] Anhui University, Hefei, China; [b] R&D Department, Chuzhou HRM Electronic Technology Co., Ltd, China; [c] Wuhan University, China; [d] Zeta Information Group Co., Ltd, China

Technical Session 48: General Analog-VI

Time	16:00-18:00, October 30, 2026	Venue	Qinglian Hall
Session Chair	Yibo Qiao, Zhejiang University, China		

Session Details		
16:00	0705	**A 6.48-mW 800-MS/s 12-bit Pipelined-SAR ADC Using CM Stabilized Critically Damped Ring Amplifier Assisted with Active-Inductor** **Yuchi Zhai[1], Meng Xu[1], Jinwei Wu[1], Yuekang Guo*[1], Jing Jin[1]** [1] Shanghai Jiao Tong University, Shanghai, China

16:15	2617	**A Computation-Efficient Confidence-Guided Timing-Skew Calibration for Time-Interleaved ADCs** **Lihan Yu[1], Jize Liu[1], Ke Wu[1], Yuekang Guo[1]** [1] Shanghai Jiao Tong University, China
16:30	2919	**An 18-bit 24-MS/s Flash-Assisted 4bit/cycle SAR ADC with Charge-Injection DAC** **Maxiang Wu[1], Baoyi Zheng[2], Guoao Wang[1], Zhaohang Bing[1], Jiahao Zhao[1], Tieliang Zhang[*1]** [1] Beijing Microelectronics Technology Institute, China; [2] Tsinghua University, China
16:45	5639	**A 0.6 V 94.2-dB SNDR 40-kHz BW Fully Dynamic Time-Interleaved Delta-Sigma Modulator in 180 nm CMOS** **Jun Xiao[1], Yuke Shen[1,2,*], Yi Ding[1], Jiahe Li[1], Zhong Tang[1,2], Yanbo Zhang[1,2], Yi Shen[1,2], Shubin Liu[1,2], Ruixue Ding[1,2], Zhangming Zhu[1,2]** [1] Hangzhou Institute of Technology, Xidian University, China; [2] Xidian University, China
17:00	7648	**A Charge-Domain Power-Efficient ELD Compensation Technique for CT ΔΣ Modulators** **Ziqi Gao[1], Tao Zhong[1], Meng Xu[1], Yuekang Guo*[1], Jing Jin[1]** [1] Shanghai Jiao Tong University, China
17:15	1207	**A Highly Robust 5-V/2.5-V Bandgap Reference with an Ultra-Low-Temperature-Drift Compensation Technique** **Zhao Huang[1], Xinyu Jiang[2], Manman Zhu[3], Jie Sun*[1]** Nanjing University of Aeronautics and Astronautics Nanjing, China
17:30	1535	**A 15-b ENOB 20-kHz-BW Fully Passive 2nd-Order Noise Shaping SAR ADC Achieving 182-dB FoMs** **Yiming Wang, Furong Sun, Mengdi Li, Xing Wu, Liangjian Lyu*** East China Normal University, China
17:45	3294	**A Distributed SLE Edge Recorder for Spatially Separated EEG–EMG Acquisition** **Weiqi Luo[1], Lechen Zhong[2], Yizhen Chen[1], Jian Mei[1,3], Yong Huang[1], Menglei Zhu[1], Yushan Dai[1],Yanfei Sun[1,3], Zekai Hu[4], Rui Yin*[1,3], Junyu Wang*[1]** [1] Fudan University, China; [2] The University of Hong Kong, China; [3] National Integrated Circuit Innovation Center, China; [4] Shanghai University, China

Technical Session 49: CMOS Logic Devices & Sensors-VII

Time	16:00-18:00, October 30, 2026	Venue	Huanying Hall
Session Chair	Chaoyue Zheng, Yangtze Delta Region Institute (Huzhou), University of Electronic Science and Technology of China, Huzhou, China		

Session Details

16:00	9348	**Defect Reduction and Valence Stabilization in p-Type SnO Thin-Film Transistors by Atmosphere-Dependent Dual-Step Annealing** **Guanlin Qiu, Chong Ma, Zihao Guo, Dun-Bao Ruan*** Fuzhou University, Jinjiang, China

16:15	6212	**An Adaptive MoS2-Based Schmitt Trigger for Waveform Shaping and Neuron Emulation** **Guanting Liu, Bingshuo Ding, Gaochen Yang, Jiaming Wu, Chenlong Ma, LeiTong*, LeiYe*** Huazhong University of Science and Technology, China
16:30	5488	**A Dynamic Co-Design of PUF and TRNG Exploiting Deeply-Worn 3D NAND Flash Memory** **Guoyu Wang[1], Ji Zhong[2], Pu Wang[3], Xuepeng Zhan[1], Jixuan Wu[1], Zhelong Piao[1], Jiezhi Chen[1,#]** [1] Shandong University, China; [2] Jinan Maiwei Intelligent Technology Co., Ltd., China; [3] Shandong Sinochip Semiconductors Co. Ltd, China
16:45	2463	**Research on High Temperature Performance of Gallium Nitride Heterojunction Hall Sensors Based on Different Substrates** **Kainan Wang[1], Kaiming Ma[1], Nannan Ding[1], Qingyuan Zuo[1], Jianyu Zhao[1], Huolin Huang*[1], Yung L. Liang[2]** [1] Dalian University of Technology, China; [2] National University of Singapore, Singapore
17:00	2972	**Analysis on Effects of Trench MIM Structure and Corner Curvature on Leakage Characteristics** **Xinyue Feng, Shujun Gao, Xiang Li, Renjie Zheng, Hailong You, Cong Li** Xidian University, China
17:15	1149	**Physical Modeling and Memory Mechanism Analysis of an All-2D van der Waals Floating-Gate Transistor Using TCAD Simulation** **Sicheng Liu[1], Shuyuan Yang[1], Shengxi Cai[1], Yilin Sun*[2], Zhifang Liu*[3], Dan Xie*[1]** [1] Tsinghua University, China; [2] Sun Yat-sen University, China; [3] Beihang University, China
17:30	1306	**Area-Defined Planar Gate-Injection MoS2 Floating-Gate Transistors with Tunable Volatile Relaxation** **Binshuo Ding[1], Guanting Liu[1], Gaochen Yang[1], Chenlong Ma[1], Jiaming Wu[1], Lei Tong*[1], Lei Ye*[1]** [1] Huazhong University of Science and Technology, China
17:45	5840	**Optoelectronic Neuromorphic Devices Perceiving Ultraviolet Solar-Blind Light for Encryption Applications** **Bingqi Cai[1, 2], Jinhui Li[1, 2], Xinhang Liu[1, 2], Zhuang Li[1, 2], Kun Chen[1, 2], Chen Wang*[1, 2],and Lin Chen*[1, 2]** [1]Fudan University, China; [2] National Integrated Circuit Innovation Center, China

Technical Session 50: Power Devices & Power IC-XI

Time	16:00-18:00, October 30, 2026	Venue	Yuqing Hall
Session Chair	Xin Zhou, University of Electronic Science and Technology of China, China		

Session Details

16:00	8311	**Demonstration of Strong Short-Circuit Withstand Capability in 650-V p-GaN Gate HEMT** **Yunhong Lao[1], Teng Li[1], Sihang Liu[1], Qian Zheng[1], Jingjing Yu[1], Junjie Yang[1], Jiawei Cui[1], Han Yang[1], Qimeng Jiang[2], Gaofei Tang[2], Jin Wei*[1]** [1] Peking University, China; [2] Cloud Semi Co., Ltd, China
16:15	4037	**Origin of Dynamic RON Degradation in p-GaN Gate HEMTs at Characteristic Switching Frequency** **Bowen Huo[1], Yi Zhang[1], Wanjun Chen[1,2], Bo Zhang[1] and Ruize Sun[1,2,*]** [1] University of Electronic Science and Technology of China, China; [2] Institute of Electronic and Information Engineering of UESTC in Guangdong, China
16:30	7299	**Experimental Investigation of Trap-Induced Degradation in β-Ga2O3 Schottky Barrier Diodes** **Zejun Jiang[1], Yuxi Wei[1*], Kaiwei Dai[1], Yan Wang[1], Jie Wei[1], and Xiaorong Luo[1,2]** [1] University of Electronic Science and Technology of China, China; [2] Chengdu University of Information Technology, China
16:45	0315	**Simulation and Experimental Study on Novel β-Ga2O3 Schottky Barrier Diodes with Guard Rings Assisted Junction Termination Extension** **Jizhong Liu[1], Jie Wei*[1], Xiangnan Li[1], Jialei Tan[1], Kaiwei Dai[1], Yuxi Wei[1], and Xiaorong Luo[1, 2]** [1] University of Electronic Science and Technology of China, China; [2] Chengdu University of Information Technology, China
17:00	1364	**Mechanisms of Proton Irradiation-Induced Electrical Degradation in p-GaN Gate HEMTs** **Shuting Wang, Dongyang Wang, Mingmin Huang*, Yao Ma, Zhimei Yang, Yun Li** Sichuan University, China
17:15	7836	**An Output-Capacitance Deep-level Transient Spectroscopy (DLTS) Method for Characterizing Buffer Traps in p-GaN HEMTs Under Substrate Bias** **Jianlang Liao, Chuan Song, Shuai Zou, Peng Wu and Wen Yang*** South China University of Technology, China
17:30	4108	**A Novel Digital-biased Multi-island P-GaN HEMT for Dynamic RON Degradation Suppression** **Ruize Sun[1,2,*], Jianpeng Liu[1], Bowen Huo[1], Buwei Gu[1], Wanjun Chen[1], and Bo Zhang[1]** [1] University of Electronic Science and Technology of China, China; [2] Institute of Electronic and Information Engineering of UESTC in Guangdong, China
17:45	3537	**Temperature-Dependent Capacitance-Voltage and Interface-State Characterization of Polarization Enhanced p-GaN MIS Capacitors** **Shichao Wang[1#], Teng Li[2#], Hengyuan Qi[2], Jingjing Yu[2], Shihao Lu[1], Xufang Zhang[1*], and Jin Wei[2*]** [1] North China University of Technology, China; [2] Peking University, China

Technical Session 51: RF & Wireless-V

Time	16:00-18:00, October 30, 2026	Venue	Huiyuan Hall
Session Chair	Tong Lin, Southeast University, China		

Session Details		
16:00	6674	**A Broadband, High-Efficiency, and High-Gain GaN MMIC Power Amplifier for 5G/6G Applications** **Xinbo Zhou, Pengfei Jiang, Qu Zhang, Shudong Huo, Yunzhao Shi, Kui Dang*, Jincheng Zhang*** Xidian University, China
16:15	2484	**A Millimeter-Wave High-Linearity Up-Conversion Mixer with Spurious Suppression Technique** **Shujie Sun[1,2], Qingxuan Wei[1], Hao Wei[1], Kuan Bao[3], Jun Zhou[3], Jing Jin*[1], Jianjun Zhou[1]** [1] Shanghai Jiao Tong University, China; [2] Nanjing Electronic Devices Institute, China; [3] Nanjing Guobo Electronics Co. Ltd, China
16:30	5169	**A 57-61 GHz CMOS Receiver for Rader Detection Application** **Xincong Wang*, Ji Dong, Fei He, Ziqiang Li, Pengkun Fan, Haonan Dang** Chongqing GigaChip Technology Co. Ltd, China
16:45	2424	**A Compact 80–100 GHz 5-bit Digital Step Attenuator in 65-nm CMOS Technology** **Bo Fu[1], Lili Li [2], Xiao Ding*[1], Xuesong Han[1]** [1] University of Electronic Science and Technology of China, China; [2] National University of Defense Technology, China
17:00	8826	**A Long-Lifetime Temperature Sensor Based on Level-Crossing SAR ADC in 180-nm CMOS** **Yangtao Hu, Yuxin Tong, Xiaoliang Ji, Haidong Chang, Zhang Bin, Siwan Dong*, Huimin Du** Xi'an University of Posts and Telecommunications, China
17:15	3580	**A Low-Power Crystal-Free Digital Baseband WuR Design for Ambient IoT with Wide SFO Tolerance** **Tuo Hu[1], Qiang Li[1], Haoyu Jiang[1], Luode Chen[1], and Hao Min*[1,2]** [1] Shanghai Quanray Electronics Co., Ltd., China; [2] Fudan University, China
17:30	3149	**DC and High-Frequency Characteristics of Thin-Barrier Si-Based GaN HEMTs at Cryogenic Temperatures** **Xiaosa Gu*, Jiejie Zhu*, Qing Zhu, Wanshuo Liao, Yichong Ding, XiaoHua Ma** Xidian University, China
17:45	8573	**GaN-based X-Band Multi-function Core Chip Phase Shifter for Phased Array Radar Systems** **Muhammad Imran Nawaz[1], Mudassir Ali*[1], Erdem Aras[2], Salahuddin Zafar[1], Nasir Mohyuddin[1], Sajid Baloch[1],Ekmel Ozbay[2]** [1] Centres of Excellence in Science and Applied Technologies (CESAT), Pakistan; [2] Bilkent University, Turkey

Technical Session 52: Device Reliability & Security-VII

Time	16:00-17:30, October 30, 2026	Venue	Yaxu Hall
Session Chair	Chao Liu, Shandong University, China		

Session Details		
16:00	4909	**Trace-Mask Cache: A Page-Triggered LLC Defense Against Flush+Reload Attacks** **Donglai Zhou, Ying Zhang, Yuan Chen, Hai Yang, Yekang Chang, Rongkun Su and Xin Chen** Nanjing University of Aeronautics and Astronautics, China
16:15	4130	**Impact of Transient Dose Rate Effect on the Reliability of FD-SOI and FinFET-Based SRAM Physical Unclonable Functions** **Jinjin Shao[1], Ruiqiang Song*[1], Peipei Hao[2], Yang Guo[1], Yaqing Chi[1], Bin Liang[1], Jianjun Chen[1], JingyanXu[2], Yaohua Wang*[1]** [1] National University of Defense Technology, Changsha, China; [2] Northwest Institute of Nuclear Technology, China
16:30	0589	**Impact of Gate Width on Hot Carrier Degradation in n-Type Vertical Nanosheet Field-Effect Transistors** **Bocheng Yang[1,2], Jiao Chen[1,2], Zhicheng Wang[1,2], Fang Wang[1,2], Qianqian Liu[1,2], YongkuiZhang*[1,2], Xiaolei Wang[1,2], Jun Luo[1,2], Hong Yang*[1,2]** [1] Chinese Academy of Sciences, China; [2] University of Chinese Academy of Sciences, China
16:45	7505	**Nitridation-Dependent Defect Charge Dynamics Analysis Based on the Hi-Lo CISS-VG Method in SiC MOSFETs Under Negative-Bias HTGB Stress** **Ziming Xia[1], Zehong Li*[, 1, 2], Xin Zhang[3, 4], Zhishuo Xu[1], Anna Zhang[3], Hao Wang[3], Shuaibing He[1],Yisheng Yu[1], Tongyang Wang[1], Yige Zheng[1], Zhaoqing Jin[1], Xuan Wang[1], Li Xiao[3], Min Ren[1, 2]** [1] University of Electronic Science and Technology of China, China; [2] Chongqing Institute of Microelectronics Industry Technology, University of Electronic Science and Technology of China, China; [3] China Resources Microelectronics, China; [4] Fudan University, China
17:00	4238	**New Compact Model for Transient Thermal Coupling Prediction in Advanced BEOL Interconnect Structures** **Xuhan Wang, Shuying Wang, Pengpeng Ren*, Zhigang Ji** Shanghai Jiao Tong University, China
17:15	5956	**Anomalous NBTI Degradation Investigation on Logic 8V PMOSFET Device** **Xiong Li, Huijuan Zhu, Xueyong Yao, Wenxing Tian, Zhiwei Wang, Yuhan Ju, Xiong Li*** iRay Image Technology (Hefei) Company, China

Technical Session 53: Semiconductor Process Technologies-III

Time	16:00-17:30, October 30, 2026	Venue	Shuibo Hall
Session Chair	Weifeng Lv, Hangzhou Dianzi University, China		

Session Details		
16:00	7415	**High-Uniformity and Versatile Ohmic Contact on P-Type 4H-SiC Based on Ni/Ti/Al Metallic Stack with Low-Temperature Annealing** **Qingling Li[1,2], Jiajun Dong[2], Decai Liu[2], Rui Wang[2], Tao Zhu*[1,2]** [1] University of Electronic Science and Technology of China, China; [2] Beijing Institute of Smart Energy, China
16:15	6002	**Intelligent Fault Detection Based on Machine Learning Technologies for Semiconductor Manufacturing** **Yunrui He[1,2], Ankuan Ji[2], Dedong Han*[1], Zezhong Wang[2], Xiaofeng Wang[2], Weiyang Yang[2], Lin Cui[2], Yan Sun[2]** [1] Peking University, China; [2] NAURA, China
16:30	6604	**Dual-mode Volatile/Nonvolatile Artificial Synapse Based on α-In_2Se_3/WSe_2 Van der Waals Heterostructure Transistor** **Jiyang Xu†[1], Ouwen Zhang†[1], Xinhao Zhai[1], Huajun Sun*[1], Chuqian Zhu[1], Junming Zhang[1], Ming Zeng[2], Changtian Cao[1], Daiyang Jiang[1], Yuanbing Wang[2] and Xiangshui Miao[1]** [1] Hubei Key Laboratory of Advanced Memories, China; [2] Yangtze Memory Technologies Co., Ltd., China
16:45	2402	**Effect of Doping Geometry on the Two-Dimensional Electron Gas in AlGaAs/InGaAs/GaAs Heterostructures: Symmetric Quantum Well versus MODFET** **Bowen Shen[1], Yang Cao[1], Yingwei Yuan[2], Yue Wang[2], Zexi Huang[2], Aynul Islam*[1]** [1] Nanyang Technological University, Singapore; [2,*1]Glasgow College, University of Glasgow, UESTC, China
17:00	5027	**Superlattice Engineering of Enhanced Hafnia Piezoelectricity via Dual Regulation of Grain Size and Interfacial Stress** **Chuqian Zhu†[1], Jiyang Xu†[1], Huajun Sun*[1], Junming Zhang[1], Ming Zeng[2], Changtian Cao[1], DaiyangJiang[1], Yuanbing Wang[2] and Xiangshui Miao[1]** [1] Huazhong University of Science and Technology, China; [2] Yangtze Memory Technologies Co., Ltd., China
17:15	2961	**Li-Doped AlOx/In2O3 Synaptic TFTs with Electrically Erasable Multilevel Conductance for 5×5 Array Emulation** **Ruohan Li†, Yitian Li†, Yiwen Wang†, Junxu Tao, Yanming Kuang, Shuge Wang, and Chun Zhao*** Xi'an Jiaotong-Liverpool University, China

Technical Session 54: Digital Architectures & Systems-IV

Time	16:00-18:00, October 30, 2026	Venue	Tianhan Hall
Session Chair	Zhuoer Li, Zhejiang University, China		

Session Details

16:00	9684	**TAILOR: Tail-Latency-Aware Transaction Shaping and Memory-Locality Co-Optimization for LLM Decode-Stage KV Cache Access over PCIe/CXL** **Huiyang Yu, Junyu Lin, Ning Chen, Lei Shen*** Fudan University, China
16:15	1167	**Design of a Resource-Sharing Fixed-Point Complex Multiplier Based on RISC-V Instruction Extension** **Mingrui Hao, Zhenyu Wu*, Haiyan Chen, Xiaowen Chen** National University of Defense Technology, China
16:30	1285	**RAFA: A Posit-Based Reconfigurable Activation Function Architecture** **Shiyu Peng, Fen Ge*, Zhuo Li** Nanjing University of Aeronautics and Astronautics, China
16:45	6879	**Artificial Intelligence Chip Design for Accelerating Hyperdimensional Computing** **Haojiang Bai[1], Shenjian Zhang[2], Yuxiao Fang[1], Zongjie Shen[1*], Chun Zhao[1*], Jiaqi Liu[1*]** [1] Xi'an Jiaotong-Liverpool University, China; [2] The Hong Kong University of Science and Technology, China
17:00	1730	**Hardware-Efficient Physics-Constrained Dynamic Programming for Robust Doppler Estimation in LEO-IoT Receivers** **Zhigang Zhou[1]*, Yi Fang[1], Huajie Yu[1], Yunzhou Qiu[2*]** [1] Hangzhou Dianzi University, China; [2] Shanghai University of Electric Power, China
17:15	7581	**An Efficient Unified Hardware Architecture for Softmax and LayerNorm in Transformers** **Tianxing Xie, Zifeng Zhao, Jiewen Zheng, Gengsheng Chen, Wenbo Yin*** Fudan University, China
17:30	6076	**U2A2: Uncertainty-Triggered Adaptive Avoidance for Event-Camera UAVs** **Xuming Zhang†, Chao Zhang†, Letian Jia, Junyi Han,Yujie Huang*, Minge Jing*, Xiaoyang Zeng*** Fudan University, China
17:45	8021	**ZOLAI-Q: A Loop-Aware Fused Instruction Queue for Low-Power VLIW/DSA Front Ends** **Zhouhe Zhang and Xuehong Lin*** Beijing University of Posts and Telecommunications, China

Poster Session

Poster Session 01

15:30-16:00, October 28, 2026 @Foyer(1F)

Board No.	Paper ID	Paper Details
P01	0210	**Design Space Exploration of Array-level 1T1C Structure FeRAM for Performance Optimization** **Fangzheng Zhang[1], Huanning Zhang[1], Can Liu[1], Xiguang Wu[1,2], Wei Mao[1,2], Xiao Yu[1,2], Bing Chen[1,2], Bo Li[1,2*], Xiao Yu[3], Yan Liu[1,2], Genquan Han[1,2]** [1]Hangzhou Institute of Technology, Xidian University, China; [2] Xidian University, China; [3] Zhejiang Zentel Memory Technology Co, Ltd., China
P02	6529	**AlScN-based Ferroelectric Memcapacitor For Neuromorphic Computing and Logic-in-Memory Operations** **Wenxin Sun[1], Xihui Yuan*[1, 2], Ruiqing Wang[1], Zhe Chen[2], Siying Zheng[1, 2], Haiwen Xu[1, 2], BochangLi[1, 2], Bing Chen[1, 2], Jiuren Zhou*[1,2], Yan Liu[1, 2], Yue Hao[1, 2], and Genquan Han[1, 2]** [1] Xidian University, China; [2] Hangzhou Institute of Technology, Xidian University, China
P03	7539	**Total Ionizing Dose Effects on FeFET-based Reconfigurable NAND/NOR Logic Gate** **Yulin Zhang[1], Huan Liu[1,2,*], Zheng Zhang[1], Peiyuan Du[1], Fei Yu[1,2], Yong Wang[1], Xiao Yu[1,2], YanLiu[1], Yue Hao[1], Genquan Han[1,2]** [1] Xidian University, China; [2] Hangzhou Institute of Technology, Xidian University, China
P04	3887	**Gate-Stack-Dependent Ga2O3 Capping for Selective PBTI Suppression in Vertical IGZO Transistors** **Yuting Chen, Gangping Yan, Lu Tai, Xinlv Duan, Liguo Chai, Yongqing Shen, Zhiyu Tian, Chuqiao Niu, Xueli Ma*, Jinjuan Xiang*, Guilei Wang, Chao Zhao** Beijing Superstring Academy of Memory Technology, China
P05	3846	**Memory-Aware Fused Polynomial Instructions for Unified Kyber–Dilithium Acceleration** **Hongbo Feng[1], Mingbo Wang[1], Yong Zhang[2], Fan Zhang[2], Siyuan Chen[1], Jiahao Lu[1,3], Hao Li[1], Ang Hu[1,3], and Dongsheng Liu[1,3]** [1]Huazhong University of Science and Technology, China; [2] Hubei Siant Science & Technology Co., Ltd., China; [3] JinYinHu Laboratory, China
P06	0480	**Design and Implementation of Control Scheduling Mechanism for MCCSIP-RAA Based on Task List and Special Scheduling Instructions** **Longmei Nan*, Yu Jin, Yiran Du, Wei Li, Yanjiang Liu, Lin Chen, Tao Chen, Xiaoxiao Zheng** Information Engineering University, China

P07	2432	**A Schmitt-Trigger PUF with Dual-Mode Initialization for Double Entropy Extraction** **Jian Cai, Mengfan Xu, Yuejun Zhang*** Ningbo University, China
P08	2826	**GCS-Curve Candidate-Gating Front End for Edge Intelligent UAV Power-Line Sensing** **Chao Zhang[1,†], Xuming Zhang [1,†], Letian Jia[1], Junyi Han[1],Yujie Huang*[,1], Minge Jing*[,1], Xiaoyang Zeng*** Fudan University, China
P09	6470	**DRER: Enforce DRAM Runtime Error Resistance By Bias In Large Language Model Inference** **Yonghong Xiao, Yi Kang*** University of Science and Technology of China, China
P10	2947	**An Edge AI-Oriented High-Efficiency Hybrid Alignment Dual-Mode FP CIM Macro** **Yifan Zhang[1], Ye Lin[1], Chongkang Tan[2], Li Du[1], Dawei Li*[3], Yuan Du*[1]** [1] Nanjing University, Nanjing, China; [2] Ant group, Hangzhou, China; [3] Wuhan University of Technology, China
P11	4448	**A Scheduling Method for Multiple CNNs on Multi-Chiplet Accelerator Architecture** **Mingxiu Xie, Congfeng Lv, Fen Ge*** Nanjing University of Aeronautics and Astronautics, China
P12	8084	**Design and Multiphysics Optimization of a V-Shaped Thermal Actuator for In-Situ Fracture Characterization of Silicon Thin Films** **Md Sadan Hossain Ratul*, Md Al Shahriar Akash, Tian-Yu Geng, Zai-Fa Zhou*** Southeast University, China
P13	0672	**Fast Electro-Thermal Modeling of Power Electronic Devices Based on Nonlinear Discrete Green's Function** **Yiyang Chen[1], Yihong Liang[1], Yuqiao Zhang[2], Bo Zhang[1], Yourun Zhang*[1]** [1] University of Electronic Science and Technology of China, China; [2] Gree Electronic Appliances, Inc. China
P14	7337	**Quantum Correction Simulation of the FinFET Short-Channel Effect Under the Influence of Interface Traps** **Dongxv Xiao[1], Yuchen Qiu[1], Xingyv Liu[1], Pan Xinxin*[1], and Benfu Jiang*[1]** [1] Zhuhai College of Science and Technology, China
P15	6981	**MLU: A Machine Learning-based Adaptive LU Factorization Solver Selection Framework for Fast Transient Simulation** **Siyuan Cheng[†1], Zhengzhuo Wang[†2], Nan Zhan[1], Yunchu Li[2], Qingyi Shao*[1], Jianguo Hu*[2,3]** [1] South China Normal University, China; [2] Sun Yat-sen University, China; [3] Shenzhen Research Institute of Sun Yat-Sen University, China
P16	1112	**SeriWrap: A Zero-Intrusion I/O Wrapping Framework for FPGA Accelerators** **Zhaochen He, Jianrong Zhang, Yuhang Cheng , Lingli Wang*** Fudan University, China

P17	0201	**A DC-72.7 GHz Amplifier with Transformer-Peaking Stagger-Compensation Technique in 65-nm CMOS Process** **Yanjun Ma, Peiling Li, Weiping Wu** Hunan University, China
P18	9001	**A Wideband Modified Asymmetric Marchand Balun Based on Three-Coupled-Line Structure** **Zeyi Wang, Wavelet Wang, Yinsheng Bian, Qi Zhang, Peng Zhao, Member, IEEE** Hangzhou Dianzi University, China
P19	0058	**A 5-14 GHz Wideband Power Amplifier With 36-dBm Psat and 33% PAE in 0.25-μm GaN** **Shitao Li[1], Mengru Yang*[1], Xiangxi Yan [2]** [1] Nanjing University of Aeronautics and Astronautics, China; [2] Purple Mountain Laboratories, China
P20	8423	**A mmWave Digital Step Attenuator With AI-Aided Interstage Matching and Phase Calibration** **Liming Rao, Jinfan Liang, Shengfan He, Lei Zhang*** Tsinghua University, China
P21	2294	**A 92–96 GHz SPST Electronic Switch Based on HISL and GaAs Schottky Diodes** **Menghan Li, Shixiong Liang*, Yi Wu, Yang Yu, Ming Yin, Binbin Ma, Wenyu Yan, Ding Ma** Tianjin University, China
P22	4007	**A 10.7-12.6 GHz Low-Phase-Noise Differential Common-Collector Colpitts VCO in 180-nm BiCMOS** **Yu Xiao, Kaiyang Kang, Peng Gao*, Pufeng Chen, Xudong Wang** Nankai University, China

Poster Session 02

15:30-16:00, October 29, 2026 @Foyer(1F)

Board No.	Paper ID	Paper Details
P01	8987	**A Three-Stage High-Efficiency GaN HEMT Power Amplifier with Harmonic Termination Assisted Matching** **Ke Liu, Xijun Huang, Jing Xiao*, Kai Tang** Hunan University, China
P02	3311	**79–83 GHz Open-Loop FMCW Frequency Synthesizer Using a Class-F VCO in 28-nm FD-SOI CMOS** **Arvind Singh Rawat*, Yann Deval, Herve Lapuyade, Francois Rivet** University of Bordeaux, France7

P03	0051	**A 0.72 pJ/bit 48-Gb/s PAM-4 Transmitter Combining Quarter-Rate iPWM Equalization and Passive CTLE for XSR Interconnects** **Chen Wang, Huzhi Tang, Yuekang Guo, Hao Wei, Jing Jin*** Shanghai Jiao Tong University, China
P04	9337	**A 28-Gbaud PAM-4/NRZ Dual-Mode Transmitter in 65-nm CMOS** **Chaoping Wu, Jian Yang, Danna Wu, Xiyao Li, Fa Dai, Liping Zhong*** Guangdong University of Technology, China
P05	9475	**A Low-Power Time-Interleaved Noise-Shaping SAR ADC Based on VCO Quantizer** **Junfeng Tang, Xian Tang*** Shenzhen International Graduate School, Tsinghua University, China
P06	8855	**A 20-MSPS High-Precision Isolated ADC for Server Power-Supply Protection** **Xiaowei Zhang** Zhejiang University, China
P07	0006	**An Isolated Differential Charge Amplifier with Time-Division-Multiplexing Clock Synchronization for Integrated Isolated DC-DC Converters** **Guanzhi Chen[1, 2], Jiahui Liu[1], Shaowei Zhen[1,*], Zuyue Pang[1], Dongmin Ding[2], Bo Zhang[1]** [1] University of Electronic Science and Technology of China, China; [2] CR Microelectronic, China
P08	7325	**A High Speed DAH PWM Micro-LED Pixel Circuit Enabled by Incorporating a Cascaded Inverter** **Zixin Zhang[1], Haohang Zeng[1], Lu Chang[1], Xin Zheng[1], Congwei Liao*[2], Lei Lu[1], Shengdong Zhang*[1]** [1] Peking University, Shenzhen, China; [2] Shenzhen Technology University, China
P09	4605	**A Column-Parallel TS-SAR ADC with Cumulative Probability Difference Calibration of Specific Codes for CMOS Image Sensor** **Ming Ouyang[1], Lixiang Han[2], Hao Li[1], Jun Xiu[3] , Ang Hu[1]*** [1] Huazhong University of Science and Technology, China; [2] Huazhong University of Science and Technology, China; [3] Neusoft Corporation Shenyang, China
P10	4861	**Design and Analysis of a Gain-Reconfigurable Wideband Analog Front-End** **Lingxin Zeng[1,2], Bingjun Xiong[1,2], Jiajun Huang[1,2], Chunlin Ji[3], Jingjing Liu*[1,2]** [1] Sun Yat-sen University, Shenzhen, China; [2] Guangdong Provincial Key Laboratory of Sea-Air-Space Communication, China; [3] Kuang-Chi Institute of Advanced Technology, China
P11	2683	**A 54MSps, 14 Bit Pipeline-SAR ADC Using PVT Robust Ring Amplifier and Non-binary Redundant SAR ADC** **Yutong Zhang[2], HaiTao Meng[2], XueJing Liu[2], HongDa Zhang[2], HanJun Jiang[1], Yan Chen*[1 2]** [1] Tsinghua University, China; [2] CEC Huada Electronic Design Co., Ltd., China

P12	2863	**A 105.5-dB SNDR, 24-kHz BW Discrete-Time Zoom ADC With a Passive Noise-Shaping SAR ADC** **Jiawei Zhang[1,2], Xuan Guo[1], Linzhen Wu[1], Hanbo Jia[1], Ming Chen*[1]** [1] Chinese Academy of Sciences, China; [2] University of Chinese Academy of Sciences, China
P13	3858	**A Low-Jitter Synchronization Clock Architecture for TI-Pipelined ADCs in 28nm CMOS** **Tao Liu[1,2], Zhengfei Li[2], Ruiqi Yang[1,2], Xuan Guo*[1] , Hanbo Jia[1] , Kai Sun[1], Xinyu Liu[1]** [1] Institute of Microelectronics of the Chinese Academy of Sciences, China; [2] University of Chinese Academy of Sciences, China
P14	6180	**A High-Speed Low-Power Dynamic Comparator with Cross-Coupled Preamplification** **Zijie Wang[1], Cuixia Wang*[1]** Tongji University, China
P15	9260	**A 10-bit SAR ADC With a Compact Analog Multiplexer for Multi-Channel Biomedical Acquisition** **Zengqing Liang†[1], Xianzhao Li†[1], Yuezhong Chen[1], Jianming Xu[1], Quanzhen Duan[1], Georges Gielen[2], Xinpeng Xing*[1]** [1] Sun Yat-sen University, China; [2] KU Leuven, Belgium
P16	9932	**An I/Q Calibration Circuit with 0.005°Phase Accuracy Achieving 65.74dB IRR** **Changbo Xu [1], Gan Wang [2], Mingyong Xin [1], Houyi Zhang [1], Xu Wu *[2,3]** [1] Electric Power Research Institute of Guizhou Power Grid Co., Ltd. Guiyang, China; [2] Southeast University, China; [3] Purple Mountain Laboratories, China
P17	6799	**A 250-MS/s 9-bit VTC/TDC-Assisted SAR ADC With TDC Reuse for Metastability-Based Resolution Enhancement** **Zhiyang Zhao[1], Jiayi Chen[1], Yuekang Guo*[1], Jing Jin[1], Jianjun Zhou[1]** [1] Shanghai Jiao Tong University, China
P18	3220	**A 1.9% Undershoot 12V-to-1V DSD Converter with Phase-Adaptive Adjustment** **Jie Wang[1], Lei Chen[1], Zhenyuan Zhang[1], Xiaoyang Xue[1], Ze Gao[1], Zirui Li[1], Yimeng Zhang[1,2]*, Yuming Zhang[1,2]** [1] Xidian University, China; [2] Key Laboratory of Analog Integrated Circuits and Systems (Xidian University), Ministry of Education, China
P19	1067	**A 340ppm/℃, 0.2%/V PVT-Insensitive Constant gm Current Bias with On-Chip Calibrated Resistors** **Yuting Wan, Kexin Shan, Jiaqing Rui, Xing Wu, Liangjian Lyu*** East China Normal University, China
P20	1998	**An On-Chip Triangular Current Frequency Modulator for Constant On-Time Buck Converters** **Shaohua Peng[1], Zhaonian Yang*[1], Xinru Liu[1], Xinyu Lv[1], Shiguang Li[1], Huangzhang Xu[2]** [1] Xi'an University of Technology, China; [2] Xi'an Zhixin Microelectronics Co. Ltd., China

P21	5160	**Novel Multi-Trench-Zone JTE for Enhanced Breakdown Performance in Fabricated 4H-SiC MOSFETs** **Yiru He[1], Yadong Huang[1], Maojiu Luo[2], Bo Zhang[1], Yourun Zhang[*1,3]** [1] University of Electronic Science and Technology of China, China; [2] Gree Electric Appliances, Inc., China; [3] Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, China
P22	1406	**Ambipolar Floating-Gate Neuromorphic Transistor Based on WSe2** **Zirui Zhang, Ce Li, Ruitong Bie, Linfeng Sun*** Beijing Institute of Technology, China

Poster Session 03

10:15-10:45, October 30, 2026 @Foyer(1F)

Board No.	Paper ID	Paper Details
P01	6770	**Repair-Trace Reuse for Source-Anchored Analog Process Migration** **YUHE WANG[1,+], WENJUN HUANG[1,+], SHENGZHI SHEN[1,+], JIALIANG REN[3],JIAKAI PAN[1],ZHENGZHUO WANG[1], YUNCHU LI[1], JIANGUO HU*[,1,2]** [1] Sun Yat-sen University, China; [2] Shenzhen Research Institute of Sun Yat-Sen University, China; [3] South China Normal University, China
P02	7467	**A Pipelined SAR ADC With Bit-Weight Calibration Exploiting Comparator Metastability Detection** **Haodong Pu[1], Meng Xu[1], Yuekang Guo*[1,2], Jing Jin[1,2]** Shanghai Jiao Tong University, China
P03	0415	**A 100MHz-BW Pipelined Noise Shaping ADC with VTV-assisted Error-Feedback** **Shizhan Mo, Mingqiang Guo*** University of Macau, China
P04	4183	**A 512-Channel Analog Front-End Readout IC for InGaAs Linear Spectrometry Sensor** **Beichen Zhao[1,†], Yixiao Hu [1,†], Shuangyu Lyu[1], Ting Yi[1], Jian Mei*[1,2]** [1] Fudan University, China; [2] National Integrated Circuit Innovation Center, China
P05	6658	**A Multi-Path Multi-Level Distributed Regulated Reference Circuit for AMOLED Source Drivers to Suppress Dynamic AC Noise** **Zhifeng Mao[1,2], Wei Liu[1], Bin Sheng[1], Fei Gou[1], Jing Xie[1], Wenwei Xu[1], Jun Xu*[2]** [1] Glenfly Tech Co., Ltd., China; [2] Tsinghua University, China
P06	1935	**Asymmetric Performance Variations in Monolithic CFETs Induced by Gate Sidewall Angle** **Xiaoyu Cheng[1], Xu Cheng[2], Xiaoxu Kang, Zetong Chen, Tianci Miao[1], Qihang Zheng[1] , Kaiyuan Zhao[1], Zurong Xie, Xin Zhang, Shengwu Li[1], and Kailin Ren[1*]** [1] Shanghai University, China; [2] Fudan University, China

P07	3348	**Low-Temperature Annealing Induced Interfacial Redox Modulation in TeOx/IGZO All-Oxide pn Heterojunctions** **Qiliang Lai[1], Zihao Guo[1], Zhibo Zeng[1], Xiaolin Jiang[1], Dun-Bao Ruan[1,2,*]** [1] Fuzhou University, Fuzhou, China; [2] Fuzhou University, Jinjiang, China
P08	1187	**A Monolithic CMOS MEMS Thermopile Infrared Sensor: Design, Thermal Interference Modeling, and Validation** **Jiagen Cheng[1], Wanli Jiang[2], WeiHuang Yang[1], Yu Gao[1], Chaoran Liu[1], Dehui Xu[2], Linxi Dong*[1]** [1] Hangzhou Dianzi University, China; [2] Other R&D Department Shanghai Ye Ying Microelectronics Technology Co., Ltd., China
P09	9774	**Physics-Guided Prediction of RRAM Current Degradation in Endurance Cycling** **Chengyu Liu, Zongwei Wang*, Shuai Hu, Yujie Chen, Lin Bao, Ling Liang, Yimao Cai** Peking University, China
P10	7989	**A Novel DTFET for Ternary Inverter Applications** **Bin Lu[1], Linlin Xing[1], Guoqiang Chai[1], Jiayu Di[1*], Yanfei Hu[2*]** [1] Shanxi Normal University, China; [2] Xidian University, China
P11	6930	**A Stacked Graphene-MoS2 Temperature-Gradient Gate for Thermophoretic Control in Silicon Nitride Nanopores** **Candong Zhao[1], Guangyi Yang[1], Hantao Jia[1], Yuanbin Chen[1], Huangsheng Peng[1], Fuwei Zhuge[2], Xiangshui Miao[1], Yuhui He*[1]** [1] Huazhong University of Science and Technology, China; [2] Huazhong University of Science and Technology, China
P12	2295	**Revisiting the Influence of Oxide Thickness and Its Random Variations on Tunnel FETs** **Yunhe Guan*, Renjie Liu, Tongqing Yan, Haotong Han, Xiangtai Liu, Haifeng Chen** Xi'an University of Posts & Telecommunications, China
P13	6048	**TCAD Study of Interface-Trap-Assisted Ferroelectric Switching and Memory Characteristics in HZO-Based FeFETs** **Yong-Qi Zhou, Haijiao Harsan Ma*, Jincheng Zhang** Xidian University, China
P14	5695	**A Compact Model for Amorphous IGZO TFT Including Both Interface Trap Charges and Channel Thickness** **Chunsheng Jiang[1,2], Cong Li[1,2], Qin Xie[1,2,*]** [1] Guangxi Normal University, China; [2] Guangxi Universities Engineering Research Center for Optoelectronic Information Technology, China
P15	2741	**TCAD-Resolved Defect-State Engineering in Ultrathin IWO Thin-Film Transistors via H_2O_2-Assisted Supercritical CO_2 Treatment** **Chong Ma[1], Zihao Guo[2], Zhibo Zeng[2], Dun-Bao Ruan[1,2,*]** [1] Fuzhou University, Jinjiang, China; [2] Fuzhou University, Fuzhou, China

P16	1663	**Research on a Data-Augmentation-Based Neural-Network Model Methodology for Electrical-Parameter Prediction of 40nm MOSFETs** **Fan Yang[1,2], Jun Zhou[2], Tiantian Shi[1], Zerui Jin[1], Fanxiang Shen[1], Xiaoli Ji[*1]** [1] Nanjing University, China; [2] Wuhan Xinxin Semiconductor Manufacturing Co., Ltd., China
P17	4467	**High-Transconductance Buried-Channel PMOS with Optimized Well and Channel Doping for Low-Noise Analog Circuits** **Yongshun Li[1,2], Teng Liu[1,2], Rongshuo Liu[1], An Sun[2], Huajun Jin[2], Liang Song[2], Nailong He[2], SenZhang[2], Wentong Zhang[1*] and Bo Zhang[1]** [1]University of Electronic Science and Technology of China, China; [2] CSMC Technologies Corporation, China
P18	5126	**Geometry and Process Parameter Screening of 5 nm Nanosheet GAAFETs Toward 3 nm FinFET Performance** **Chunxin Li, Yang Shen*, Botong Zhao ,Peng Liu, Hua Qiang, Jiahao Wang, Bingyi Ye, Yuhang Zhang, Xiaojin Li, Changyong Xiao, Yabin Sun*** East China Normal University, China
P19	1616	**SiC/β-Ga2O3 E-mode Vertical MOSFET With Integrated Reverse-conducting Schottky Barrier Diode** **Wen Bo[1], Jialei Tan[1], Heng Sun[1], Kaiwei Dai[1], Yuxi Wei*[1], Jie Wei*[1], and Xiaorong Luo[1, 2]** [1] University of Electronic Science and Technology of China, China; [2] Chengdu University of Information Technology, China
P20	8730	**Double RESURF Structure Automated Design Using Dual Simulated Annealing Algorithm under Design Constraint** **Hongbin Gao[1,2], Jing Chen*[1,2], Man Li[1,2], Kemeng Yang[1,2], Jun Zhang[1,2], Jiafei Yao[1,2], Yufeng Guo*[1,2]** [1] Nanjing University of Posts and Telecommunications, China; [2] National & Local Joint Engineering Laboratory for RF Integration and Micro-Packaging Technologies, China
P21	7712	**A Novel Junction-Controlled-Diode Assisted Split-Gate SiC MOSFET** **Huimin Ma, Xuan Li *, Ziye Deng, Jingchao Yuan, Jinggui Zhou, Xiaochuan Deng, Bo Zhang** University of Electronic Science and Technology of China, China
P22	5230	**A Hall Sensor Interface Featuring > 149 dB Notch Depth SCNF and 110 nT/√Hz EIN Density** **Lishuang Lin[1,2], Qingzhen Xu[2], Hua Fan[2,3,*], Jiangchao Wu[4]** [1]Chengdu Sino Microelectronics Technology Co., LTD, Chengdu, China; [2]University of Electronic Science and Technology of China, China; [3]Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, Shenzhen, China; [4]University of Macau, China

Poster Session 04

15:30-16:00, October 30, 2026 @Foyer(1F)

Board No.	Paper ID	Paper Details
P01	0007	**A High Performance and Unified Reed-Muller Decoder for HQC** **Xianqi Mei[1], Jiahao Lu*[1], Tianze Huang[1], Dongsheng Liu[1], Jiawei Liang[1], Ang Hu[1]** [1]Huazhong University of Science and Technology, China
P02	7333	**Multi-Objective DC-DC Converter Optimization via GA-BP Cascaded Residual Network and NSGA-II Clustering** **Xingsen Chen[1], Shikai Sun[2], Xincai Liu[1], Xufeng Liao[1], Lianxi Liu[1]** [1]Xidian University, China; [2]Beijing Microelectronics Technology Institute, China
P03	4275	**TCAD Study of a Superjunction GaN HEMT Bidirectional Switch** **Ze Zhang[1], Qingyuan Zuo[1], Yun Lei[1], Liangju Guo[1], Huolin Huang*[1], Yung L. Liang[2]** [1]Dalian University of Technology, China; [2]National University of Singapore, Singapore
P04	7596	**An On-chip Local Voltage Sensor for 1200 V 4H-SiC MOSFET Based on Controllable Electron Barrier** **Shuaibing He[1], Yang Yang[1, 2], Zehong Li[*, 1], Ziming Xia[1], Zhishuo Xu[1], Yisheng Yu[1], Min Ren[1]** [1]University of Electronic Science and Technology of China, China; [2]China Resources Microelectronics (Chongqing) Limited, Chongqing, China
P05	3208	**Surrogate-Assisted Robust Screening of Floating Field Limiting Ring Termination Under Surface-Charge Deviation** **Zixuan Cheng[1], Zhiwei Jin[1], Haimeng Huang*[1]** [1]Glasgow College, University of Electronic Science and Technology of China, China
P06	8260	**A Reference-Defined Pre-Bias Scheme with Bandgap-Referenced Pre-Regulator and A Transient-Enhanced HV-LDO for GaN Gate Drivers** **Gefu Wang[1], Jiatong Wu[1], Xufeng Liao[1,2] and Lianxi Liu*[1,2]** [1]Xidian University, China; [2]Xidian University Chongqing ICs Innovation Institute, Xiyong Microelectronics Park, China
P07	6406	**Novel Termination with Schottky Contact for Suppressing Minority Carrier Injection in SiC MOSFET** **Wenjie Jiang[1,2], Yun Xia*[1], Changwei Zheng[1], Wei Liu[1], Menglong Zhang[1], Gang Chen[1], Yuxi Wan[1], Xiaochuan Deng[2]** [1] Shenzhen Pinghu Laboratory, China; [2]Shenzhen Institute for Advanced Study, UESTC, Shenzhen, China
P08	2554	**A Digital LDO with Voltage-Time Dual-Domain Regulation Based on a High-Linearity VTC** **Jingying Yuan, Pengjun Wang, Handong Lu, Ruonan Pei, Hao Ye*** Wenzhou University, China
P09	8443	**A 1200-V SiC Lateral Monolithic Bidirectional Switch with Shared RESURF Drift Region for Power ICs** **Hangyuan Yu[1], Yijiang Liu[1], Yan Wang*[1]**

		[1]Tsinghua University, China
P10	6970	**p-GaN HEMTs with Al_2O_3/a-Si Stacked Passivation for Simultaneous Suppression of Dynamic ON-Resistance Degradation and Threshold Voltage Shift** **Yujie Lei[1], Cheng Yu[2], Guojian Ding[2], Haiqiang Jia[2,3], Miao He[*1], Yang Wang[*2]** [1]Guangdong University of Technology, China; [2] Songshan Lake Materials Laboratory, China; [3]China Academy of Sciences, China
P11	0819	**A Low-Cost Approximate Time-Optimal Digital Controller with Hysteretic On-Off Duty Compensation for DC-DC Converters** **Bingwei Wang[1,2], Shuyan Zhu[1,2]*, Qinwei Lai[3], Shaolin Liao[1], Yunchu Li[1,2]** [1]Sun Yat-sen University, China; [2]Zhuhai Key Laboratory of Millimeter-wave Terahertz Antenna and RFIC, SYSU, Zhuhai, China; [3]AMICRO Semiconductor Co., Ltd., China
P12	4360	**Novel Data-Efficient AI Model via Active Learning on SOI LDMOS and Its Experiments** **Ying Xiang[1], Teng Liu[1,2] Nailong He[2], Zhenyan Liu[1], Shengyuan Wang[1], Yiduo Xie[1], Liqi An[2],Yongshun Li[1,2], Huajun Jin [2], Sen Zhang[2], Wentong Zhang[1*] and Bo Zhang[1]** [1]University of Electronic Science and Technology of China, China; [2]CSMC Technologies Corporation, China
P13	1355	**Optimization Study of the Square Cell Structure in SiC Superjunction VDMOSFET** **Yizhen Zhao[1], Hao Yuan*[1], Wenhan Yang[1], Fei Tong[1], Yu Zhou[1], Fengyu Du[1], Chao Han[1],Xiaoyan Tang[1], Qingwen Song[1], Yuming Zhang[1]** [1]Xidian University, China
P14	9496	**Module-Level Configuration-Fault Criticality Analysis of FPGA CNN Accelerators for Selective Hardening** **Jingyu Wang[1], Shanqiang Yang[3], Chenxu Wang*[1,2], Tianliang Xu[1], Zhenbin Lv[3], Liang Han[1], MinLuo[1], Yuhang Wang[3]** [1]Harbin Institute of Technology, Weihai, China; [2]Key Laboratory of Cross-Domain Synergy and Comprehensive Support for Unmanned Marine Systems, Ministry o f Industry and Information Technology, Weihai, China; [3]Harbin Institute of Technology, Harbin, China
P15	7468	**Dual-Chain Hashing Authentication JTAG Architecture for Chiplets** **Yuan Chen[1], Ying Zhang[1], Donglai Zhou[1], Hai Yang[1], Rongkun Su[1], Yekang Chang[1] and Fang Zhou[1]** [1]Nanjing University of Aeronautics and Astronautics, China

P16	4192	**HfO_2/ZrO_2 Superlattice Ferroelectric Thin Films: Fabrication and Characterization** **Yi Song[1,2], Chen Xia [1,2], and Chunsheng Jiang*[1,2]** [1]Key Laboratory of Integrated Circuits and Microsystems (Guangxi Normal University), Education Department of Guangxi Zhuang Autonomous Region, Guilin, China; [2]Guangxi Universities Engineering Research Center for Optoelectronic Information Technology, China
P17	4686	**Optimization of PMOSFET Performance in 22 nm Process via SiGe Source/Drain Technology** **Huasong Liu, Luqiao Yin*** Shanghai University, China
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